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M6117D : 386SX Embedded Microcontroller

Section 1 : Introduction

The M6117D is a highly integrated, low voltage, single-chip implementation of Intel • ™ 386SX compatible microprocessor plus ALi• M1217B chipset. The M6117D provides the following functions : 1) Intel™ 386SX core 2)Supports EDO DRAM controller including FP mode 3) Coprocessor Interface 4) ISA interface 5) Peripheral Interface (includes two cascaded 8237 DMA controllers, a 74612 memory mapper, 2 cascaded 8259 interrupt controller, and an 8254 programmer counter 6) Built-in RTC 7) Programmable 2 channels chip select 8) Built-in PS2 Keyboard Controller and Mouse 9) Built-in WATCHDOG timer 10) 16-bits GPI/O via SD bus and 16-bits independent GPIO 11) IDE interface .

The following sections highlight the main features and functions of the M6117D chip. For additional information, see Section 3 of this data sheet.

1.1 Features and Functions

■ **Static Intel 386SX compatible Core**

- Operating Power Supply 5.0V
- Operating frequency 25Mhz to 40Mhz

■ **Memory Controller**

- Supports EDO DRAM
- Supports on board memory size up to 16M bytes for 386SX or 64M bytes upgrade system using 256K, 512K, 1M, 4M or 16M SIMMs
- Supports up to 4-bank DRAM interface
- Page interleave DRAM access for FP mode
- Programmable shadow RAM from A to B segment in 128K byte and C to F segment in 32K byte unit
- Provides "RAS only" refresh or "CAS before RAS" refresh types
- Parity generation and checking

■ **Peripheral Interface**

- Includes 2 cascaded 8237 DMA controllers
- Includes 1 74612 memory mapper
- Includes 2 cascaded 8259 interrupt controllers
- Includes 1 8254 programming counter

■ **ISA Interface**

- Executes cycles for requests from CPU, DMA and ISA bus master
- Assembles or de-assembles data for multiple bus cycle or unmatched data width
- Generates refresh signals to ISA slots during DRAM refresh cycles

■ **Built-in RTC**

- Internal Real Time Clock that provides 128 byte CMOS RAM

■ **Programmable 2 channels chip select**

- Provide chip select for memory or I/O device without external address decode random logic

■ **Built-In PS2/AT Keyboard Controller**

- Internal PS2/AT keyboard controller and mouse

■ **PMU interface**

- Supports CPU SMM mode, SMI feature
- Supports APM control
- Provides External Suspend mode switch
- Provides four (4) system states for power saving (On, Doze, Standby, Suspend)
- Supports RTC alarm wake up control

■ **Expandable GPI/O signals**

- Provides sixteen External power control input and output signals
- Provides sixteen independent pin for general purpose input and output signals

■ **Watchdog timer**

- When timer times out , a system reset or NMI or IRQ happens

■ **IDE interface**
- Provides a decoder for external IDE connection

■ **Packaging**
- 208-pin PQFP package

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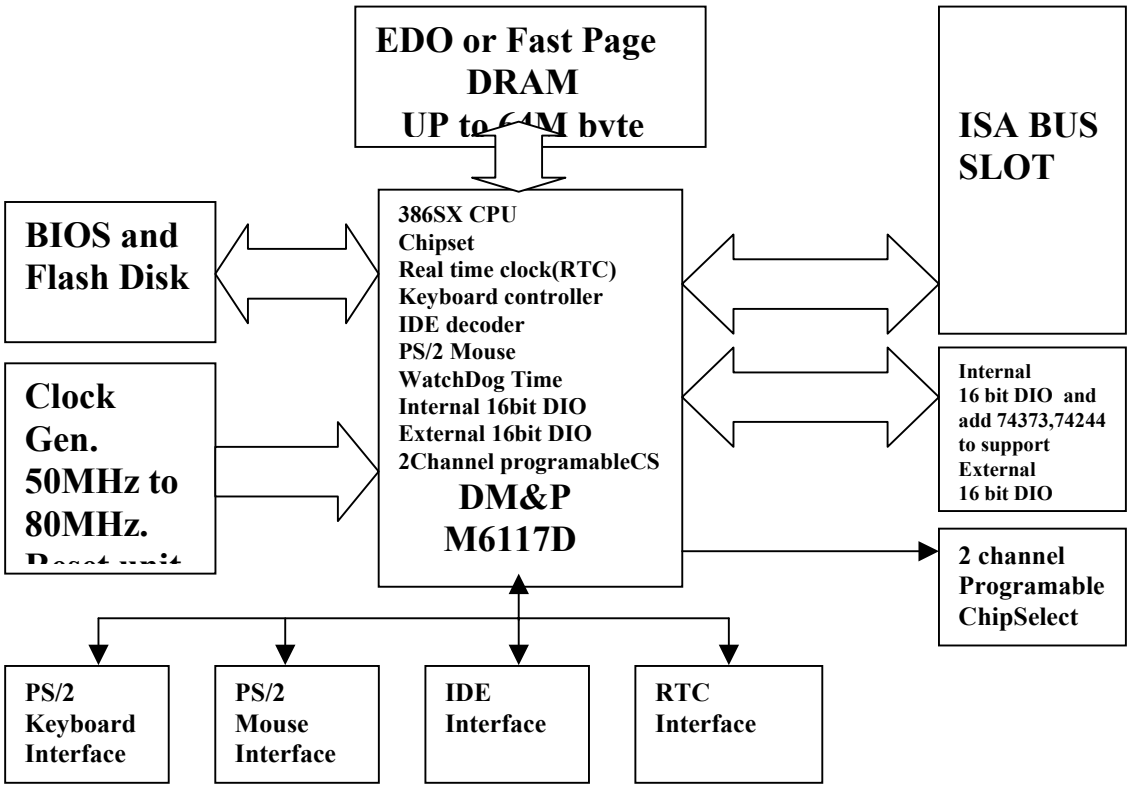
1.2 System Block Diagram



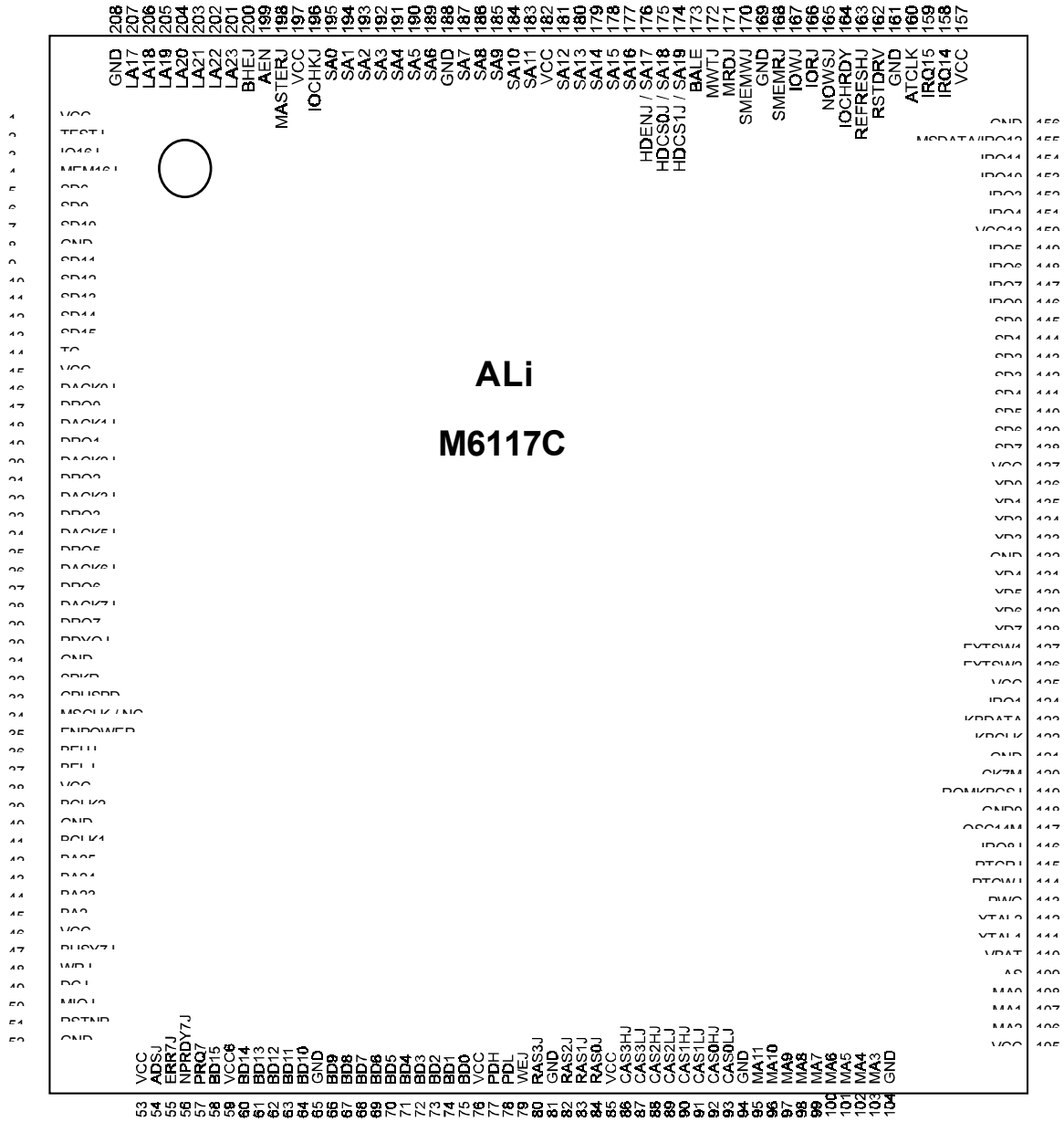
1.3 Virtue :

(a) Single Chip PC to instead 8051 or other DSP product.
(b) Easy software development, like Assembly, C, Pascal, BASIC, or Bacth file…etc.
(c) Less component to use .
(d) Support quick boot BIOS .
(e) Support free X-DOS platform .

Section 2 : Pin Description

The M6117D don't need modify any circuitry can be 100% instead ALi M6117C.
M6117D mode and M6117C mode have 22 pin difference. The M6117D pin 16 (DACK0) add a pull down 4.7K ohm resister to active M6117D mode (Default is M6117C mode).

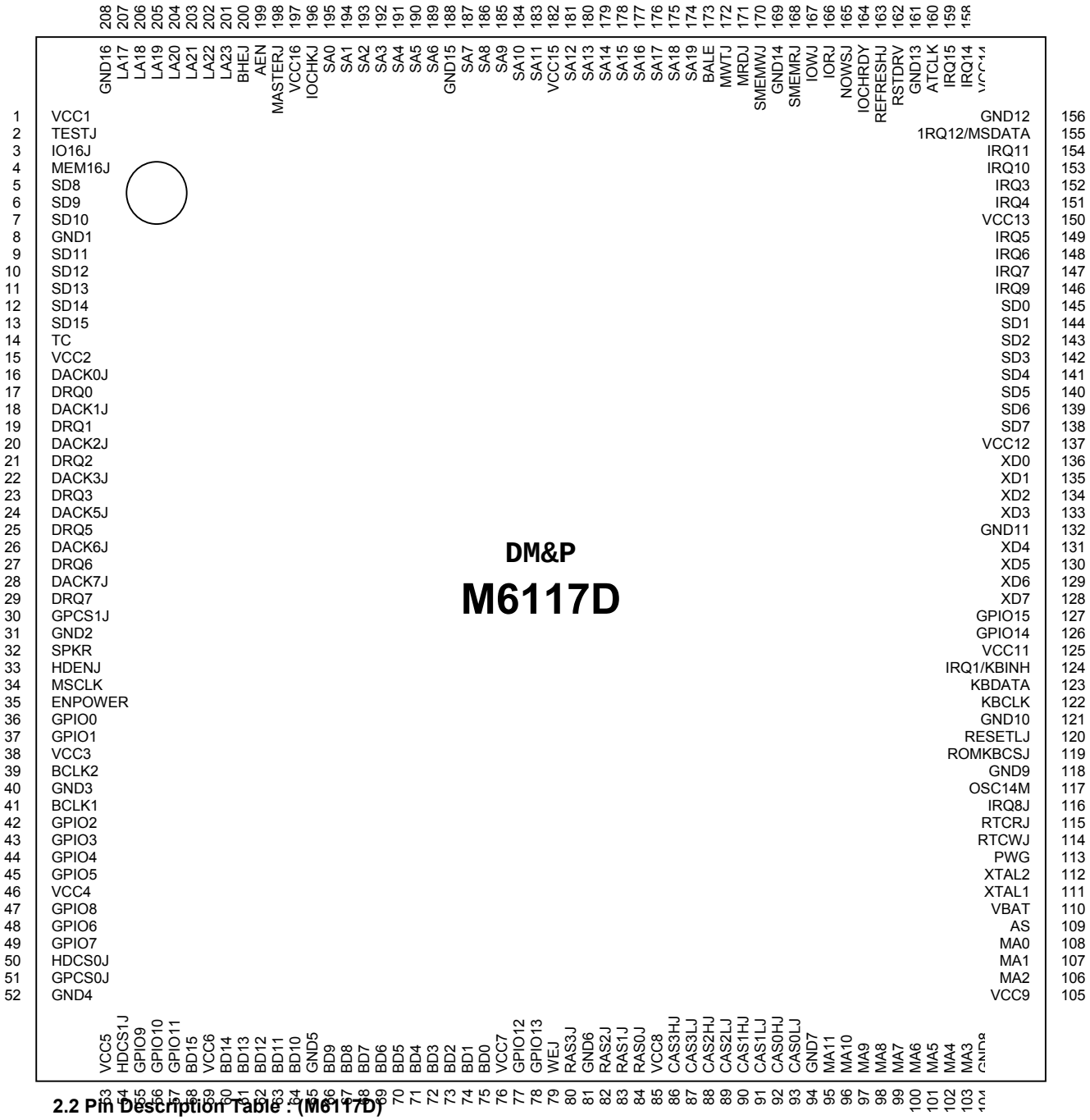
2.1 Pin Diagram (M6117C) :



2.1.1 Pin Diagram(M6117D):

M6117D mode and M6117C mode have 22pin difference. The M6117D pin 16 (DACK0) add a pull down 4.7K ohm resister to active M6117D mode (Default is M6117C mode).
M6117D more M6117C add functions list:

1. Stand-along support IDE interface.
2. 16 bit general purpose input and output pin.
3. 2 channel programmable chip select.
4. ISA slot Reset DRV inverter RESETL output.



2.2 Pin Description Table : (M6117D)

All pins are 5V TTL compatible

Pin name	Type	Pin no.	Description
Clock & Reset interface :			

PWG	I	113	**Power Good**. This indicates that the system power is enough to maintain system integrity. It resets the system when the power is low.
BCLK2	I	39	**CPU-bus Clock Input**. This is the clock input source for the internal circuit. The clock source should be the same as the CPU clock.
OSC14M	I	117	**14.318 MHz Oscillator**. This frequency is 12 times the frequency used to clock the 8254 timer counter.
ATCLK	O	160	**System Clock Output**. This signal clocks the ISA bus.
RSTDRV	O	162	**Driver Reset**. This output signal is driven active during system power up.
BCLK1	O	41	**1X CPU-bus Clock**. This is the clock divided by BCLK2.
RESETLJ	O	120	**Driver Reset LOW ACTIVE Output**. This signal reset low active when M6117D .
ISA Bus interface :			
SD[15-0]	I/O	13-9, 7-5, 138-145	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
SA[16-0]	I/O	177-181 183-187 189-195	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
SA[17]	I/O	176	ISA slot address bus for 62-pin slot.
SA[18]	I/O	175	ISA slot address bus for 62-pin slot.
SA[19]	I/O	174	ISA slot address bus for 62-pin slot.
LA[23-17]	I/O	201-207	**ISA latched address bus**. These are input signal during ISA master cycle.
IO16J	I	3	ISA 16-bit I/O device select indicator signal.
MEM16J	I	4	ISA 16-bit memory device select indicator signal.
MASTERJ	I	198	**ISA master device active signal**. ISA master access indicator signal.
MRDJ	I/O	171	**ISA memory read**. This signal is an input during ISA master cycle.
MWTJ	I/O	172	**ISA memory write**. This signal is an input during ISA master cycle.
AEN	I/O	199	**ISA I/O address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
IOCHRDY	I	164	**ISA system ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles.
BALE	O	173	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
NOWSJ	I	165	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
IOCHKJ	I	196	**ISA parity error**. M6117D will generate NMI interrupt when this signal is asserted.
BHEJ	I/O	200	**ISA byte high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
IORJ	I/O	166	**ISA I/O read**. This signal is an input during ISA master cycle.
IOWJ	I/O	167	**ISA I/O write**. This signal is an input during ISA master cycle.
SMEMRJ	O	168	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1M byte address.
SMEMWJ	O	170	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1M byte address.

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Pin Description Table - M6117D (continued) :

Pin name	Type	Pin no.	Description
REFRESHJ	I/O	163	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
Interrupt Unit :			
IRQ[7-3], IRQ[10-9], IRQ[11], IRQ[15-14]	I	147-149 151-153 146, 154, 159-158	**Interrupt request signals**. These are interrupt request input signals.
DMA Unit :			
DRQ[7-5], DRQ[3-0]	I/O	29, 27,25, 23, 21,19, 17	**DMA device request**. These are DMA request input signals.
DACK[7-5]J, DACK[3-0]J	I/O	28, 26,24, 22, 20,18, 16	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
TC	O	14	**DMA end of process**. This is the DMA channel terminal count indicating signal.
Power Management Unit :			
ENPOWER	O	35	**Enable power pin**. This active high signal updates the status of external switch.
Timer Unit :			
SPKR	O	32	**Speaker output**. Speaker data.
IDE Interface :			
HDCS0J	O	50	**HD chip select 0**. This is the hard-disk chip select 0 low active signal.
HDCS1J	O	54	**HD chip select 1**. This is the hard-disk chip select 1 low active signal.
HDENJ	O	33	**HD enable control signal**. Dedicated buffer output enable control pin for IDE bus when IDE function enable .
GPIO pins:			
GPIO[0-1]	I/O	36, 37	**Expand GPIO signals.** This signal is flexible used for customer to assert . When OE is disable , it only would be as input pin.
GPIO[2-5]	I/O	42-45	**Expand GPIO signals.** This signal is flexible used for customer to assert . When OE is disable , it only would be as input pin.
GPIO[6-7]	I/O	48-49	**Expand GPIO signals.** This signal is flexible used for customer to assert . When OE is disable , it only would be as input pin.
GPIO[8-11]	I/O	47,55-57	**Expand GPIO signals.** This signal is flexible used for customer to assert . When OE is disable , it only would be as input pin.
GPIO[13-12]	I/O	78-77	**Expand GPIO signals.** This signal is flexible used for customer to assert . When OE is disable , it only would be as input pin.
GPIO[15-14]	I/O	127, 126	**Expand GPIO signals.** This signal is flexible used for customer to assert . When OE is disable , it only would be as input pin.
DRAM Interface:			
BD[15-0]	I/O	58, 60-64 66-75	**Local data bus**. These signals are used for data transfer between local bus and DRAM interface.
RAS[3-0]J	O	80, 82-84	**RAS[3-0]J** allows eight on board DRAM SIMM slots. The detail memory configuration refers to the memory configuration table. DRAS bus signal function when Z64 mode.
CAS[3-0][HL]J	O	86-93	**CAS[n]HJ** is the CAS signal to memory bank n for high byte , **CAS[n]LJ** is the CAS signal to memory bank n for low byte. Total memory bus width is 16 bits .
WEJ	O	79	WE is the **write enable** signal to the DRAM.
MA[11:0]	O	95-103 106-108	**Memory address bus**. DRAM multiplex ROW/COLUMN address.

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Pin Description Table - M6117D (continued)

Pin name	Type	Pin no.	Description
X-bus Interface :			
ROMKBCSJ	I/O	119	**KB or ROM chip select**. Must be pulled low for normal operation.
XD[7-0]	I/O	128-131, 133-136	**X-bus data**. External bus data lines, for keyboard, BIOS ROM, RTC.
External CMOS RAM interface:			
AS	O	109	**RTC Address strobe**. This signal is used to demultiplex the address/data bus of the RTC
RTCWJ	O	114	External real time clock write strobe, active low signal.
RTCRJ	O	115	External real time clock read strobe, active low signal.
IRQ8J	I	116	**Interrupt request**. This signal is from external RTC
VBAT	I	110	**Internal RTC battery**. This must be connected to RTC battery supply when internal RTC is enabled.
XTAL1,XTAL2	I	111, 112	These pins are connected to the 32.768K crystal when internal RTC is used.
Keyboard interface:			
KBCLK	I/O	122	Keyboard interface CLK.
KBDATA	I/O	123	Keyboard interface DATA.
IRQ1/KBINH	I/O	124	**KB inhibit input** (when enable internal keyboard)/ IRQ1 input (when enable external keyboard).
Mouse interface:			
MSCLK / NC	I/O	34	**Mouse interface CLK . / (In M6117B, this is not connected).**
MSDATA/ IRQ12	I/O	155	**Mouse interface DATA / IRQ12 input .**
Miscellaneous :			
TESTJ	I	2	**Test**. This signal is used for ASIC testing, and must be pulled high during normal operation.
General purpose chip select:			
GPCS1J	O	30	**Programmable chip select 1 channel**. This drives the general purposechip select output by program the dedicated I/O or Memory area.
GPCS0J	O	51	**Programmable chip select 0 channel**. This drives the general purposechip select output by program the dedicated I/O or Memory area.
Power pins :			
VCC	1, 15, 38, 46, 53, 59, 76, 85, 105, 125, 137, 150, 157, 182, 197		**VCC.** 5.0V supply.
VSS	8, 31, 40, 52, 65, 81, 94, 104, 118, 121, 132, 156, 161, 169, 188, 208		**VSS**. Ground.

2.3 Numerical Pin List : M6117D

*** Pull high or pull low normal resister from 10K to 40K ohm.**

Pin No.	Pin Name	I/O	Cell Type	Ioh/Iol	internal pull
1	VCC1	P	IO VDD		Double bound
2	TESTJ	I	I_TTL		pull_high
3	IO16J	I	I_TTL		pull_high
4	MEM16J	I	I_TTL		pull_high
5	SD8	B	I_TTL/O_CMOS	8/16 mA	pull_high
6	SD9	B	I_TTL/O_CMOS	8/16 mA	pull_high
7	SD10	B	I_TTL/O_CMOS	8/16 mA	pull_high
8	GND1	P	IO GND		Double bound
9	SD11	B	I_TTL/O_CMOS	8/16 mA	pull_high
10	SD12	B	I_TTL/O_CMOS	8/16 mA	pull_high
11	SD13	B	I_TTL/O_CMOS	8/16 mA	pull_high
12	SD14	B	I_TTL/O_CMOS	8/16 mA	pull_high
13	SD15	B	I_TTL/O_CMOS	8/16 mA	pull_high
14	TC	O	O_CMOS	6/8 mA	pull_high
15	VCC2	P	M1386 CORE		Double bound
16	DACK0J	B	I_TTL/O_CMOS	6/8 mA	pull_high
17	DRQ0	B	I_TTL	8/16 mA	pull_low
18	DACK1J	B	I_TTL/O_CMOS	6/8 mA	pull_high
19	DRQ1	B	I_TTL	8/16 mA	pull_low
20	DACK2J	B	I_TTL/O_CMOS	6/8 mA	pull_high
21	DRQ2	B	I_TTL	8/16 mA	pull_low
22	DACK3J	B	I_TTL/O_CMOS	6/8 mA	pull_high
23	DRQ3	B	I_TTL	8/16 mA	pull_low
24	DACK5J	B	I_TTL/O_CMOS	6/8 mA	pull_high
25	DRQ5	B	I_TTL	8/16 mA	pull_low
26	DACK6J	B	I_TTL/O_CMOS	6/8 mA	pull_high
27	DRQ6	B	I_TTL	8/16 mA	pull_low
28	DACK7J	B	I_TTL/O_CMOS	6/8 mA	pull_high
29	DRQ7	B	I_TTL	8/16 mA	pull_low
30	GPCS1J	O	O_CMOS	6/8 mA	
31	GND2	P	M1386 CORE		Double bound
32	SPKR	O	O_CMOS	4/4 mA	
33	HDENJ	O	O_CMOS	4/4 mA	pull_high
34	MSCLK	B	Mouse CLOCK	12/24 mA	pull_high
35	ENPOWER	O	O_CMOS	4/4 mA	
36	GPIO0	B	I_TTL/O_CMOS	8/16 mA	pull_high
37	GPIO1	B	I_TTL/O_CMOS	8/16 mA	pull_high
38	VCC3	P	IO VDD		Double bound
39	BCLK2	I	CMOS		
40	GND3	P	M1386 CORE		Double bound
41	BCLK1	O	O_CMOS	8/16 mA	
42	GPIO2	B	I_TTL/O_CMOS	8/16 mA	pull_high
43	GPIO3	B	I_TTL/O_CMOS	8/16 mA	pull_high
44	GPIO4	B	I_TTL/O_CMOS	8/16 mA	pull_high
45	GPIO5	B	I_TTL/O_CMOS	8/16 mA	pull_high
46	VCC4	P	M1386 CORE		Double bound
47	GPIO8	B	I_TTL/O_CMOS	8/16 mA	pull_high
48	GPIO6	B	I_TTL/O_CMOS	8/16 mA	pull_high
49	GPIO7	B	I_TTL/O_CMOS	8/16 mA	pull_high
50	HDCS0J	O	O_CMOS	8/16 mA	pull_high

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Numerical Pin List : M6117D **:** *(continued)*

Pin No.	Pin Name	I/O	Cell Type	Ioh/Iol	internal pull
51	GPCS0J	O	O_CMOS	6/8 mA	
52	GND4	P	IO GND		Double bound
53	VCC5	P	IO VDD		Double bound
54	HDCS1J	O	O_CMOS	8/16 mA	pull_high
55	GPIO9	B	I_TTL/ O_CMOS	8/16 mA	pull_high
56	GPIO10	B	I_TTL/ O_CMOS	8/16 mA	pull_high
57	GPIO11	I	I_TTL/ O_CMOS	8/16 mA	pull_high
58	BD15	B	I_TTL/O_CMOS	8/16 mA	
59	VCC6	P	M1386 CORE		Double bound
60	BD14	B	I_TTL/O_CMOS	8/16 mA	
61	BD13	B	I_TTL/O_CMOS	8/16 mA	
62	BD12	B	I_TTL/O_CMOS	8/16 mA	
63	BD11	B	I_TTL/O_CMOS	8/16 mA	
64	BD10	B	I_TTL/O_CMOS	8/16 mA	
65	GND5	P	M1386 CORE		Double bound
66	BD9	B	I_TTL/O_CMOS	8/16 mA	
67	BD8	B	I_TTL/O_CMOS	8/16 mA	
68	BD7	B	I_TTL/O_CMOS	8/16 mA	
69	BD6	B	I_TTL/O_CMOS	8/16 mA	
70	BD5	B	I_TTL/O_CMOS	8/16 mA	
71	BD4	B	I_TTL/O_CMOS	8/16 mA	
72	BD3	B	I_TTL/O_CMOS	8/16 mA	
73	BD2	B	I_TTL/O_CMOS	8/16 mA	
74	BD1	B	I_TTL/O_CMOS	8/16 mA	
75	BD0	B	I_TTL/O_CMOS	8/16 mA	
76	VCC7	P	M1386 CORE		Double bound
77	GPIO12	B	I_TTL/O_CMOS	8/16 mA	pull_high
78	GPIO13	B	I_TTL/O_CMOS	8/16 mA	pull_high
79	WEJ	O	O_CMOS	12/24 mA	
80	RAS3J	O	O_CMOS	12/24 mA	
81	GND6	P	M1386 CORE		Double bound
82	RAS2J	O	O_CMOS	12/24 mA	
83	RAS1J	O	O_CMOS	12/24 mA	
84	RAS0J	O	O_CMOS	12/24 mA	
85	VCC8	P	IO VDD		Double bound
86	CAS3HJ	O	O_CMOS	8/16 mA	
87	CAS3LJ	O	O_CMOS	8/16 mA	
88	CAS2HJ	O	O_CMOS	8/16 mA	
89	CAS2LJ	O	O_CMOS	8/16 mA	
90	CAS1HJ	O	O_CMOS	8/16 mA	
91	CAS1LJ	O	O_CMOS	8/16 mA	
92	CAS0HJ	O	O_CMOS	8/16 mA	
93	CAS0LJ	O	O_CMOS	8/16 mA	
94	GND7	P	IO GND		Double bound
95	MA11	O	O_CMOS	12/24 mA	
96	MA10	O	O_CMOS	12/24 mA	
97	MA9	O	O_CMOS	12/24 mA	
98	MA8	O	O_CMOS	12/24 mA	
99	MA7	O	O_CMOS	12/24 mA	
100	MA6	O	O_CMOS	12/24 mA	

Numerical Pin List : M6117D : (continued)

Pin No.	Pin Name	I/O	Cell Type	Ioh/Iol	internal pull
101	MA5	O	O_CMOS	12/24 mA	
102	MA4	O	O_CMOS	12/24 mA	
103	MA3	O	O_CMOS	12/24 mA	
104	GND8	P	IO GND		Double bound
105	VCC9	P	IO VDD		Double bound
106	MA2	O	O_CMOS	12/24 mA	
107	MA1	O	O_CMOS	12/24 mA	
108	MA0	O	O_CMOS	12/24 mA	
109	AS	O	O_CMOS	4/4 mA	
110	VBAT	O	RTC CORE		Double bound
111	XTAL1	O	RTC 32K XTAL		
112	XTAL2	O	RTC 32K XTAL		
113	PWG	I	I_TTL/ST		
114	RTCWJ	O	O_CMOS	4/4 mA	
115	RTCRJ	O	O_CMOS	4/4 mA	
116	IRQ8J	I	I_TTL		pull_high
117	OSC14M	I	I_TTL		
118	GND9	P	RTC CORE		Double bound
119	ROMKBCSJ	B	I_TTL/O_CMOS	6/8 mA	pull_high
120	RESETLJ	O	O_CMOS	6/8 mA	
121	GND10	P	KBC CORE		Double bound
122	KBCLK	B	KBC CLOCK	12/24 mA	pull_high
123	KBDATA	B	KBC DATA	12/24 mA	pull_high
124	IRQ1/KBINH	I/O	I_TTL/O_CMOS		pull_high
125	VCC11	P	KBC CORE		Double bound
126	GPIO14	I/O	I_TTL_ST/O_CMOS	8/16 mA	pull_high
127	GPIO15	I/O	I_TTL_ST/O_CMOS	8/16 mA	pull_high
128	XD7	B	I_TTL/O_CMOS	6/8 mA	
129	XD6	B	I_TTL/O_CMOS	6/8 mA	
130	XD5	B	I_TTL/O_CMOS	6/8 mA	
131	XD4	B	I_TTL/O_CMOS	6/8 mA	
132	GND11	P	IO GND		Double bound
133	XD3	B	I_TTL/O_CMOS	6/8 mA	
134	XD2	B	I_TTL/O_CMOS	6/8 mA	
135	XD1	B	I_TTL/O_CMOS	6/8 mA	
136	XD0	B	I_TTL/O_CMOS	6/8 mA	
137	VCC12	P	IO VDD		Double bound
138	SD7	B	I_TTL/O_CMOS	8/16 mA	pull_high
139	SD6	B	I_TTL/O_CMOS	8/16 mA	pull_high
140	SD5	B	I_TTL/O_CMOS	8/16 mA	pull_high
141	SD4	B	I_TTL/O_CMOS	8/16 mA	pull_high
142	SD3	B	I_TTL/O_CMOS	8/16 mA	pull_high
143	SD2	B	I_TTL/O_CMOS	8/16 mA	pull_high
144	SD1	B	I_TTL/O_CMOS	8/16 mA	pull_high
145	SD0	B	I_TTL/O_CMOS	8/16 mA	pull_high
146	IRQ9	I	I_TTL		pull_high
147	IRQ7	I	I_TTL		pull_high
148	IRQ6	I	I_ TTL		pull_high
149	IRQ5	I	I_TTL		pull_high
150	VCC13	P	M1217B CORE		Double bound

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Numerical Pin List : M6117D : (continued)

Pin No.	Pin Name	I/O	Cell Type	Ioh/Iol	internal pull
151	IRQ4	I	I_TTL		pull_high
152	IRQ3	I	I_TTL		pull_high
153	IRQ10	I	I_TTL		pull_high
154	IRQ11	I	I_TTL		pull_high
155	IRQ12/MSDATA	B	Mouse DATA	12/24 mA	pull_high
156	GND12	P	IO GND		Double bound
157	VCC14	P	IO VDD		Double bound
158	IRQ14	I	I_TTL		pull_high
159	IRQ15	I	I_TTL		pull_high
160	ATCLK	O	O_CMOS	8/20 mA	
161	GND13	P	IO GND		Double bound
162	RSTDRV	O	O_CMOS	8/20 mA	
163	REFRESHJ	B	I_TTL/O_CMOS	8/16 mA	pull_high
164	IOCHRDY	I	I_TTL		pull_high
165	NOWSJ	I	I_TTL		pull_high
166	IORJ	B	I_TTL/O_CMOS	8/16 mA	pull_high
167	IOWJ	B	I_TTL/O_CMOS	8/16 mA	pull_high
168	SMEMRJ	O	O_CMOS	8/16 mA	
169	GND14	P	M1217B CORE		Double bound
170	SMEMWJ	O	O_CMOS	8/16 mA	
171	MRDJ	B	I_TTL/O_CMOS	8/16 mA	pull_high
172	MWTJ	B	I_TTL/O_CMOS	8/16 mA	pull_high
173	BALE	O	O_CMOS	8/16 mA	
174	SA19	B	I_TTL/O_CMOS	8/16 mA	pull_high
175	SA18	B	I_TTL/O_CMOS	8/16 mA	pull_high
176	SA17	B	I_TTL/O_CMOS	8/16 mA	pull_high
177	SA16	B	I_TTL/O_CMOS	8/16 mA	pull_high
178	SA15	B	I_TTL/O_CMOS	8/16 mA	pull_high
179	SA14	B	I_TTL/O_CMOS	8/16 mA	pull_high
180	SA13	B	I_TTL/O_CMOS	8/16 mA	pull_high
181	SA12	B	I_TTL/O_CMOS	8/16 mA	pull_high
182	VCC15	P	M1217B CORE		Double bound
183	SA11	B	I_TTL/O_CMOS	8/16 mA	pull_high
184	SA10	B	I_TTL/O_CMOS	8/16 mA	pull_high
185	SA9	B	I_TTL/O_CMOS	8/16 mA	pull_high
186	SA8	B	I_TTL/O_CMOS	8/16 mA	pull_high
187	SA7	B	I_TTL/O_CMOS	8/16 mA	pull_high
188	GND15	P	M1217B CORE		Double bound
189	SA6	B	I_TTL/O_CMOS	8/16 mA	pull_high
190	SA5	B	I_TTL/O_CMOS	8/16 mA	pull _high
191	SA4	B	I_TTL/O_CMOS	8/16 mA	pull_high
192	SA3	B	I_TTL/O_CMOS	8/16 mA	pull_high
193	SA2	B	I_TTL/O_CMOS	8/16 mA	pull_high
194	SA1	B	I_TTL/O_CMOS	8/16 mA	pull_high
195	SA0	B	I_TTL/O_CMOS	8/16 mA	pull_high
196	IOCHKJ	I	I_TTL		pull_high
197	VCC16	P	IO VDD		Double bound
198	MASTERJ	I	I_TTL		pull_high
199	AEN	B	I_TTL/O_CMOS	8/16 mA	pull_high
200	BHEJ	B	I_TTL/O_CMOS	8/16 mA	pull_high

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Numerical Pin List : M6117D **:** *(continued)*

Pin No.	Pin Name	I/O	Cell Type	Ioh/Iol	internal pull
201	LA23	B	I_TTL/O_CMOS	8/16 mA	pull_high
202	LA22	B	I_TTL/O_CMOS	8/16 mA	pull_high
203	LA21	B	I_TTL/O_CMOS	8/16 mA	pull_high
204	LA20	B	I_TTL/O_CMOS	8/16 mA	pull_high
205	LA19	B	I_TTL/O_CMOS	8/16 mA	pull_high
206	LA18	B	I_TTL/O_CMOS	8/16 mA	pull_high
207	LA17	B	I_TTL/O_CMOS	8/16 mA	pull_high
208	GND16	P	IO GND		Double bound

2.4 Alphabetical Pin List - M6117D

Pin no.	Pin name	Type
199	AEN	B
54	HDCS1J	O
109	AS	O
160	ATCLK	O
42	GPIO2	B
43	GPIO3	B
44	GPIO4	B
45	GPIO5	B
173	BALE	O
41	BCLK1	O
39	BCLK2	I
58	BD15	B
60	BD14	B
61	BD13	B
62	BD12	B
63	BD11	B
64	BD10	B
66	BD9	B
67	BD8	B
68	BD7	B
69	BD6	B
70	BD5	B
71	BD4	B
72	BD3	B
73	BD2	B
74	BD1	B
75	BD0	B
36	GPIO0	B
37	GPIO1	B
200	BHEJ	B
47	GPIO8	B
86	CAS3HJ	O
87	CAS3LJ	O
88	CAS2HJ	O
89	CAS2LJ	O

Pin no.	Pin name	Type
90	CAS1HJ	O
91	CAS1LJ	O
92	CAS0HJ	O
93	CAS0LJ	O
120	RESETLJ	O
33	HDENJ	O
16	DACK0J	B
18	DACK1J	B
20	DACK2J	B
22	DACK3J	B
24	DACK5J	B
26	DACK6J	B
28	DACK7J	B
49	GPIO7	B
17	DRQ0	I
19	DRQ1	I
21	DRQ2	I
23	DRQ3	I
25	DRQ5	I
27	DRQ6	I
29	DRQ7	I
35	ENPOWER	O
55	GPIO9	B
126	GPIO14	B
127	GPIO15	B
8	GND1	P
31	GND2	P
40	GND3	P
52	GND4	P
65	GND5	P
81	GND6	P
94	GND7	P
104	GND8	P
118	GND9	P
121	GND10	P

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Alphabetical Pin List (continued)

Pin no.	Pin name	Type
132	GND11	P
156	GND12	P
161	GND13	P
169	GND14	P
188	GND15	P
208	GND16	P
3	IO16J	I
196	IOCHKJ	I
164	IOCHRDY	I
166	IORJ	B
167	IOWJ	B
124	IRQ1/KBINH	I
151	IRQ4	I
152	IRQ3	I
116	IRQ8J	I
153	IRQ10	I
154	IRQ11	I
155	IRQ12/ MSDATA	B
146	IRQ9	I
147	IRQ7	I
148	IRQ6	I
149	IRQ5	I
158	IRQ14	I
159	IRQ15	I
122	KBCLK	B
123	KBDATA	B
201	LA23	B
202	LA22	B
203	LA21	B
204	LA20	B
205	LA19	B
206	LA18	B
207	LA17	B
95	MA11	O
96	MA10	O
97	MA9	O
98	MA8	O
99	MA7	O
100	MA6	O
101	MA5	O
102	MA4	O
103	MA3	O
106	MA2	O
107	MA1	O
108	MA0	O
198	MASTERJ	I
4	MEM16J	I
50	HDCS0J	O
171	MRDJ	B

Pin no.	Pin name	Type
172	MWTJ	B
165	NOWSJ	I
34	MSCLK (NC)	B
56	GPIO10	B
117	OSC14M	I
77	GPIO12	B
78	GPIO13	B
57	GPIO11	B
113	PWG	I
80	RAS3J	O
82	RAS2J	O
83	RAS1J	O
84	RAS0J	O
30	GPCS1J	O
163	REFRESHJ	B
119	ROMKBCSJ	B
51	GPCS0J	O
162	RSTDRV	O
114	RTCWJ	O
115	RTCRJ	O
174	SA19	B
175	SA18	B
176	SA17	B
177	SA16	B
178	SA15	B
179	SA14	B
180	SA13	B
181	SA12	B
183	SA11	B
184	SA10	B
185	SA9	B
186	SA8	B
187	SA7	B
189	SA6	B
190	SA5	B
191	SA4	B
192	SA3	B
193	SA2	B
194	SA1	B
195	SA0	B
145	SD0	B
144	SD1	B
143	SD2	B
142	SD3	B
141	SD4	B
140	SD5	B
139	SD6	B
138	SD7	B
5	SD8	B

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Alphabetical Pin List (continued)

Pin no.	Pin name	Type
6	SD9	B
7	SD10	B
9	SD11	B
10	SD12	B
11	SD13	B
12	SD14	B
13	SD15	B
168	SMEMRJ	O
170	SMEMWJ	O
32	SPKR	O
14	TC	O
2	TESTJ	I
110	VBAT	P
1	VCC1	P
15	VCC2	P
38	VCC3	P
46	VCC4	P
53	VCC5	P
59	VCC6	P
76	VCC7	P

Pin no.	Pin name	Type
85	VCC8	P
105	VCC9	P
125	VCC11	P
137	VCC12	P
150	VCC13	P
157	VCC14	P
182	VCC15	P
197	VCC16	P
79	WEJ	O
48	GPIO6	B
128	XD7	B
129	XD6	B
130	XD5	B
131	XD4	B
133	XD3	B
134	XD2	B
135	XD1	B
136	XD0	B
111	XTAL1	I
112	XTAL2	I

Note : B : Bidirectional P : Power pin
O : Output I : Input

2.5 Hardware Power-On Setup

Hardware Power-On Setup Table of M6117D

Pin No.	Pin Name	Index	Setup	Configuration
26	DACK6J	34H : D[5]	pull high	5V Vdd
22	DACK3J	34H : D[3]	pull high	M6117D mode select
20	DACK2J	34H : D[2]	pull high	Internal RTC enable
16	DACK0J	34H : D[0]	pull low	M6117D mode select. "1"= D, '0'= C mode
119	ROMKBCSJ	35H : D[7]	pull low	Normal
24	DACK5J	35H : D[6]	pull low	Normal
28	DACK7J	35H : D[5]	pull high	Internal Keyboard Controller enable
18	DACK1J	35H : D[1]	pull high	Memory parity check enable

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Section 3 : Function Description

The M6117D is designed to perform like Intel• 386SX system with deep green features. Aside from the 386SX core, it contains (1) PS2/AT Keyboard Controller and Mouse, (2) Real Time Clock to store system boot data, (3) Programmable chip select, (4) Integrated System Peripheral to serve the peripheral requests, (5) Power Management Unit to reduce the chip's power consumption efficiently, (6) LS245 : TTL data buffer between ISA data bus SD[7:0] and ROM data bus XD[7:0], (7) DRAM Controller for four banks memory module supporting EDO and Fast Page Mode with page interleave and up to 64M bytes space, (8) IDE decoder function. The M6117D offers the following blocks :

- Static 386SX Core
- Reset and Clock logic
- CPU Interface logic
- DRAM Controller
- Configuration Registers
- ISA Bus Interface logic
- Control logic
- Address Decode and Memory Mapping logic
- Data Buffer
- Address Buffer
- ISP Devices (82C37x2, 82C59x2, 82C54, 74LS612)
- Real Time Clock
- Real Time Clock interface
- PS2/AT Keyboard /Mouse Controller
- Keyboard and Speaker logic
- Parity Generation and Checking logic
- Power Management Unit
- WATCHDOG timer
- 16 bits GPIO
- IDE decoder interface
- Programmable chip select

3.1 Static 386SX Core

The 386SX core is the same as M1386SX of Acer Labs. Inc. and 100% object code compatible with the Intel 386SX microprocessor. System manufacturers can provide 386 CPU based systems optimized for both cost and size. Instruction pipelining and high bus bandwidth ensure short average instruction execution times and high system throughput. Furthermore, it can keep the state internally from charge leakage while external clock to the core is stopped without storing the data in registers. The power consumption here is almost zero when clock stops. The internal structure of this core is 32-bit data and address bus with very low supply current, 116 mA in the conditions of 5.0V, 20MHz, room temperature. Real mode as well as Protected mode are available and can run MS-DOS, MS-Windows, OS/2 and UNIX.

3.2 Reset and Clock logic

The switching power supply sends a PWG (power good signal) to M6117D to generate system reset signals, like RSTDRV, RESETL, and resets the chip to initial state. Also the reset signal can be generated by internal emulation RC reset and shutdown cycle.
There are two clock inputs: BCLK2 and OSC are 2X system clock and 14.318MHz respectively, and three clock outputs: BCLK1, ATCLK1 and CK7M which provide frequency operation for the system board and devices depending on 1X clock used. The BCLK1 is a half frequency of BCLK2. The CK7M derived from the OSC input (divided by 2) is available as the keyboard controller clock when power is on. To increase system performance, the M6117D supports variable AT clocks for faster ISA add-on cards. When the CPU accesses the register programmed special address range, the AT clock changes to a faster speed. The non-programmed address regions keep the normal speed. There are eight programmable frequencies of the ATCLK1 which can change on fly by different specific addresses and determined by D[2:0] of local port 1EH in both high and normal speed. Please refer to Section 4.2 index 1EH. This optional AT clock can achieve a higher performance when a faster add-on card is used.

3.3 Programmable Chip Select logic

For 386SX systems, M6117D generates GPCS0J, GPCS1J to support the memory or I/O device. When general purpose chip select is active, this indicated that an 15-bit channnel address and mask address are used to specify a channel's active address block. When the processor access an address in memory or I/O, the upper 15-bit address are compared to the chip-select channel address and OR'd with the channel mask. This means that the chip select until compares the channel address and ORs the channel mask to A25:A11 for memory address and A15:A1 for I/O address.

3.4 DRAM Controller

The DRAM controller supports Fast Page Mode DRAM and EDO DRAM.The DRAM controller is capable of accessing up to 64 MBytes of local memory, and supporting four banks page interleave of DRAM using 256K, 512K, 1M, 2M, 4M, 16M single sided SIMMs. Page interleave mechanism is able to shorten the memory read/write cycle and raise the data access speed between host and RAM, and works on any two banks with the same DRAM type. Each bank can be disabled through software, please refer to 4.3 memory type configuration and 4.2 index 10H. When using EDO DRAMs, only page mode are enabled. Programmable DRAM timing is provided for RAS pre-charge time and RAS-to-CAS delay to achieve highest performance and reliability, this part is described in 4.2 index 11H and 12H. And they also explain how to use the 256/384KB memory remapping feature in unshadowed

RAM region from A0000H to FFFFFH. The A0000H to BFFFFH region can set to shadow enable, please refer to index 3CH and 12H. Programmable shadowing features are supported on 32K boundaries between C0000H and FFFFFH regions (768KB..1MB), please refer to 4.2 index 14H and 15H. It also supports •AS only", •AS before RAS" refresh type of DRAMs.

3.5 Configuration Registers

The configuration register controls the whole system of the environment under different frequencies. It enables the system to set these configuration registers to meet the compatible, reliable performance and functional requirements.

3.6 ISA Bus Interface Logic

This block includes the ISA bus state machine, 16-bit or 8-bit commands justified, command wait states and control logic. These signals are compatible with PC/AT standards.

3.7 Control logic

The control logic controls the internal data bus and address bus flow. It also generates proper read-select to internal device and uses multiplexer to choose the correct data output. It selects the correct address bus for DMA and refresh cycles to send to system.

3.8 Address Decode and Memory Mapping logic

The 16-bit address decode-circuit fully decodes the BIOS ROM, keyboard controller, internal ISP devices, real time clock, port 61H, and configuration registers. When remap is enabled, it decodes the remap memory to the end of DRAM.

3.9 Data Buffer

This block generates signals which control data transfer between the CPU core data bus, memory data bus and ISA data bus during CPU cycles, ISA bus cycles, DMA cycles and master cycles. Moreover, we added LS245, TTL data buffer between ISA data bus SD[7:0] and ROM data bus XD[7:0], on the ASIC. So that users could save some external TTL logic.

3.10 Address Buffer

The address buffer generated at address SA1, SA0 and BHEJ for ISA bus, initiates the byte-enable signal at DMA and master cycles.

3.11 ISP Devices (82C37x2, 82C59x2, 82C54, 74LS612)

The integrated system peripheral (ISP) devices are built-in, thus no 82C206 is required. There are two 82C37s, two 82C59s, one 82C54 and one 74LS612 built-in devices.

Note : The function of 82C54 has some limitations, please see appendix C.

3.12 Real Time Clock

The real time clock (RTC) device is built-in, thus no external RTC is required. If the user does not use the internal RTC for something else, then it can be disabled by hardware setting, please refer to 2.5 Hardware setting.

3.13 Real Time Clock Interface logic

The M6117D provides address strobe (AS), RTC write and read (RTCWJ and RTCRJ) signals to support external ral time clcok (RTC).

3.14 PS2/AT Keyboard/Mouse Controller

The PS2/AT keyboard controller (KBC) device is built-in, and support with Mouse, thus no external KBC is required. If the user does not use the internal KBC for something else, then it can be disabled by hardware setting, please refer to 2.5 Hardware setting.

3.15 Keyboard and Speaker logic

This block emulates the keyboard controller fast-RC and fast gate-A20 functions for maximum performance. It combines with port 61H at this block to generate speaker signal.

3.16 Power Management Unit

The M6117D Power management unit includes SMM, I/O trap, APM, external SMI switch control and programmable clock timeout unit for I/O device. The PMU strictly controls and dramatically reduces overall system power consumption. This is accomplished via the activity monitors which detect the system inactivity timer timeout, and signals the power saving device to remove the power sources from various peripherals. The M6117D provides one timer from one-second to 300 minutes to monitor the system states (ON/DOZE/ STANDBY/ SUSPEND modes). The M6117D provides an LED flash control to indicate the system state status. The M6117D supports external SMI switch into suspend mode, SMI setup, and wakeup events (RTC alarm). The M6117D also provides the interaction control for SMIJ and CPURST.

3.17.1 SMM Control Logic

M6117D supports internal 386SX core SMM mode, the M6117D will record these SMI events as :

a. Time-out events :	PMU - Mode timeout
b. I/O trap events :	VGA device access harddisk device access line-printer device access General I/O port access General memory ports access

c. External device events : IRQ• active
DRQ• active
Input devices active
External suspend-switch
RTC alarm
SMI setup-switch

d. Software SMI event

3.17.2 APM

The APM (Advanced Power Management interface) creates an interface to allow the OS to communicate with the SMM code. The M6117D provides the configuration index 56H bit 6 to generate the software SMIJ signal for APM applications.

3.18 16 bits GPIO +16 sets of GPI/O power control signals

In additiion to 16 independent GPIOs , the M6117D provides 16 expandable GPOs and 16 expandable GPIs. The user can program at most 322 signals to control power, flash disk, IDE, LED… and so on application for peripheral devices. Please refer to Section 4.9.

3.19 WATCH DOG timer

The M6117D has watchdog timer function for monitoring whether the system is still work or not after a period of time. If the system happened some error or hanged up, it cause the timer timed out, then a system reset or NMI or IRQ may happen decided by BIOS programming. The WATCHDOG timer source is 32.768 Khz frequency to counter a 24 bits counter such that the timer range is from 30.5 usecs to 512 secs with resolution 30.5 usecs. Please refer to Section 4.10 .

3.20 IDE decoder interface

The M6117D adds IDE decoder interface for PIO mode signal. It provides one channel connected with external HDD by decoding SA[15:0] with two kinds of channel selectable.

	HDCS0J	HDCS1J
primary channel	1F0 - 1F7	3F6
secondary channel	170 - 177	376

Section 4 : Configuration Registers

4.1 How to read/write to configuration registers

The read/write configuration register is the first index to be processed. On board I/O port 22h is the index register and I/O port 23h is the data register. To read a configuration register, write the index value to I/O port 22h in advance, then read data from I/O port 23h. To write a configuration register, write the index value to I/O port 22h, then write data to I/O port 23h. For instance, if we want to read the data of configuration register which index is 10h, the steps are :

1) Write 10h (index) to I/O port 22h
2) Read data from I/O port 23h

If we want to write data 55h to configuration register which index is 12h, then the steps are :

1) Write 12h (index) to I/O port 22h
2) Write data 55h to I/O port 23h

*The steps of locking/unlocking the configuration registers :

```
OUT 22h, 13h   (Enable 13h)
OUT 23h, C5h   (Unlock)
OUT 22h, XXh   (XX = Configuration Index)
OUT 23h, YYh   (YY = Configuration data)
OUT 22h, XXh
OUT 23h, YYh (Configuration can be written
               repeatedly)
  :
OUT 22h, 13h   (Enable 13h)
OUT 23h, 00h   (Lock)
```

4.2 Hardware Power-On setup

Refer to Section 2.5 Hardware power on setup table.

4.3 Memory Controller

4.3.1 How to enable/disable memory controller

Memory Controller will be enabled if D[7] of index 20h is set to 1, or is disabled if reset D[7]. All original DRAM cycles (local memory cycles) will turn to ISA bus cycles when memory controller is disabled. Meanwhile, WEJ and all RAS and CAS signals are driven high when memory controller does not work. In other words, all memory access will be treated as memory accessing on ISA bus. Related timing waveforms, please refer to Section 6.

4.3.2 How to set memory mode

Memory Controller supports Fast Page Mode and EDO DRAMs. D[0] of index 37h is set to select which kind of DRAM. The default is set to 0 to select Fast Page Mode DRAM. When D[0] of index 37h is set to 1, DRAM is set to EDO DRAM. EDO and Fast Page Mode DRAMs can not mix, so only one type of DRAM can exist at the same time. See Table below. There are 32 modes of memory type configuration which supports up to six DRAM types including 256K, 512K, 1M, 2M, 4M and 16M. Moreover, various 30-pin or 72-pin single-sided SIMMs are available on system design. We also offer a memory autosizing method described by flow chart (Section 5.4 -A) to detect memory mode on board as user• reference.

Table 4-3 Memory Type Configuration

Mode	BANK 0	BANK 1	BANK 2	BANK 3	Total Space	PM(4:0)
0	256K*2	256K*2			1M Bytes	0 0 0 0 0
1	256K*2	256K*2	256K*2	256K*2	2M Bytes	0 0 0 0 1
2	256K*2	256K*2	1M *2		3M Bytes	0 0 0 1 0
3	256K*2	256K*2	1M *2	1M *2	5M Bytes	0 0 0 1 1
4	256K*2	256K*2	4M *2		9M Bytes	0 0 1 0 0
5	512K*2				1M Bytes	0 0 1 0 1
6	512K*2	512K*2			2M Bytes	0 0 1 1 0
7	512K*2	512K*2	1M *2		4M Bytes	0 0 1 1 1
8	512K*2	512K*2	1M *2	1M *2	6M Bytes	0 1 0 0 0
9	512K*2	512K*2	4M *2		10M Bytes	0 1 0 0 1
10	512K*2	512K*2	4M *2	4M *2	18M Bytes	0 1 0 1 0
11	512K*2	1M *2			3M Bytes	0 1 0 1 1
12	512K*2	1M *2	1M *2		5M Bytes	0 1 1 0 0
13	512K*2	4M *2			9M Bytes	0 1 1 0 1
14	1M *2				2M Bytes	0 1 1 1 0
15	1M *2	1M *2			4M Bytes	0 1 1 1 1
16	1M *2	1M *2	1M *2		6M Bytes	1 0 0 0 0
17	1M *2	1M *2	1M *2	1M *2	8M Bytes	1 0 0 0 1
18	1M *2	1M *2	4M *2		12M Bytes	1 0 0 1 0
19	1M *2	1M *2	4M *2	4M *2	20M Bytes	1 0 0 1 1
20	1M *2	4M *2			10M Bytes	1 0 1 0 0
21	1M *2	4M *2	4M *2		18M Bytes	1 0 1 0 1
22	1M *2	4M *2	4M *2	4M *2	26M Bytes	1 0 1 1 0
23	2M *2				4M Bytes	1 0 1 1 1
24	2M *2	2M *2			8M Bytes	1 1 0 0 0
25	2M *2	2M *2	4M *2	4M *2	24M Bytes	1 1 0 0 1
26	2M *2	4M *2			12M Bytes	1 1 0 1 0
27	4M *2				8M Bytes	1 1 0 1 1
28	4M *2	4M *2			16M Bytes	1 1 1 0 0
29	4M *2	4M *2	4M *2		24M Bytes	1 1 1 0 1
30	4M *2	4M *2	4M *2	4M *2	32M Bytes	1 1 1 1 0
31	16M *2	16M *2			64M Bytes	1 1 1 1 1

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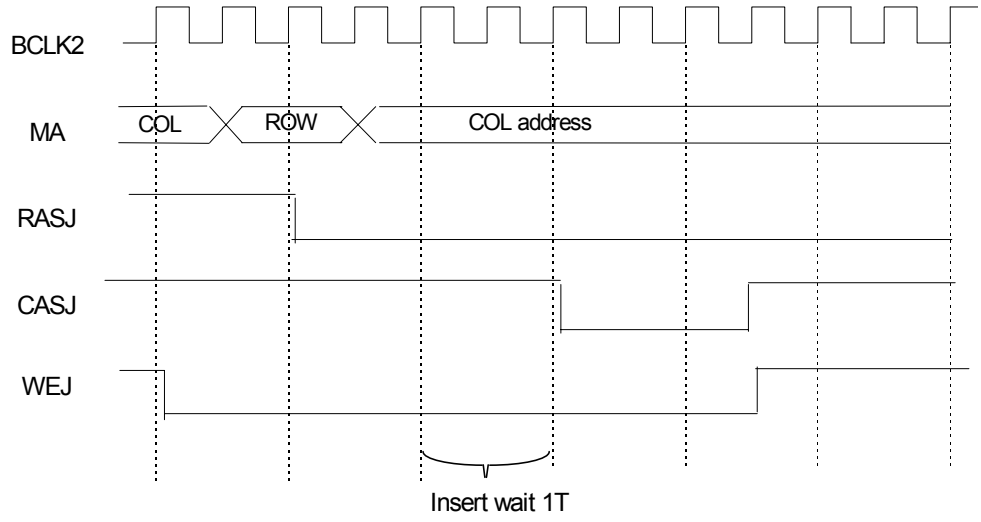
4.3.3 DRAM timing control

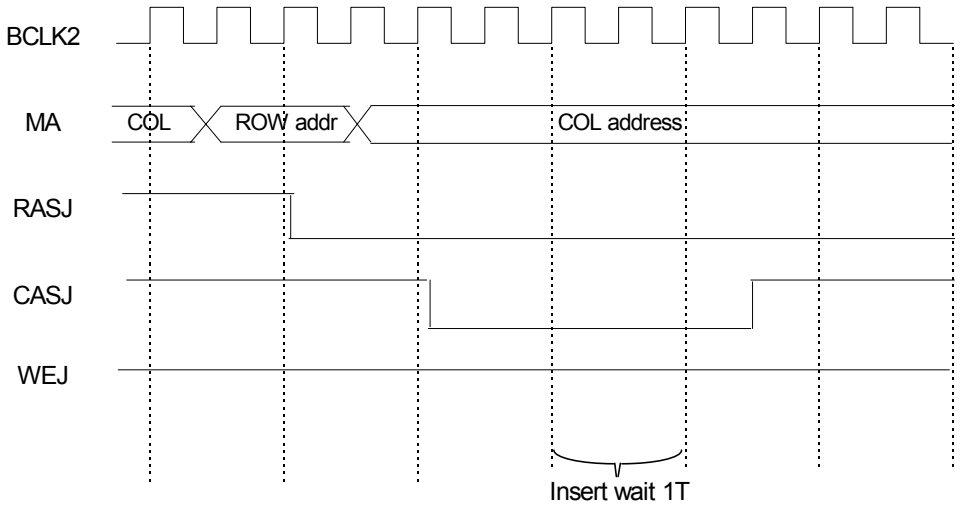
(a) Memory write access time insert wait

CASJ precharge time (high time) will last for one more T-cycle before its falling edge if D[7] of index 11h is set to high.



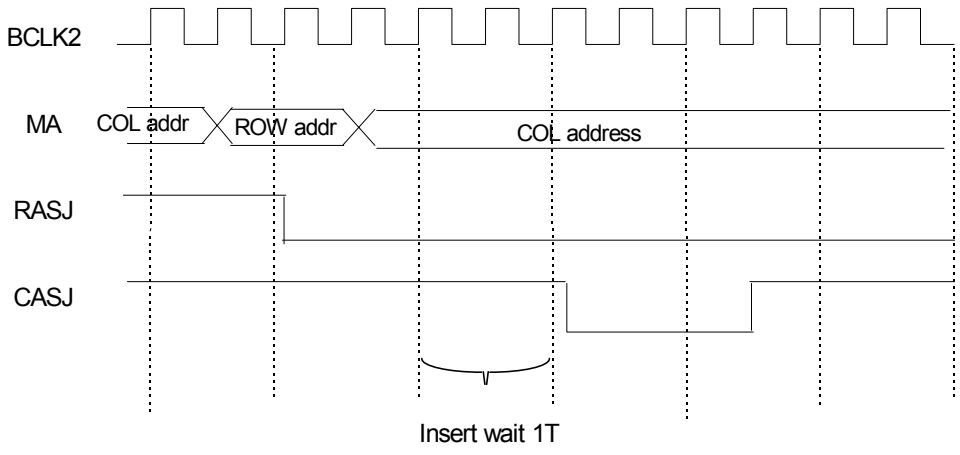
(b) Memory CAS read access time insert wait

When memory read cycles. CASJ active time (low time) will last for one more T-cycle before its rising edge if D[6] of index 11h is set to high.



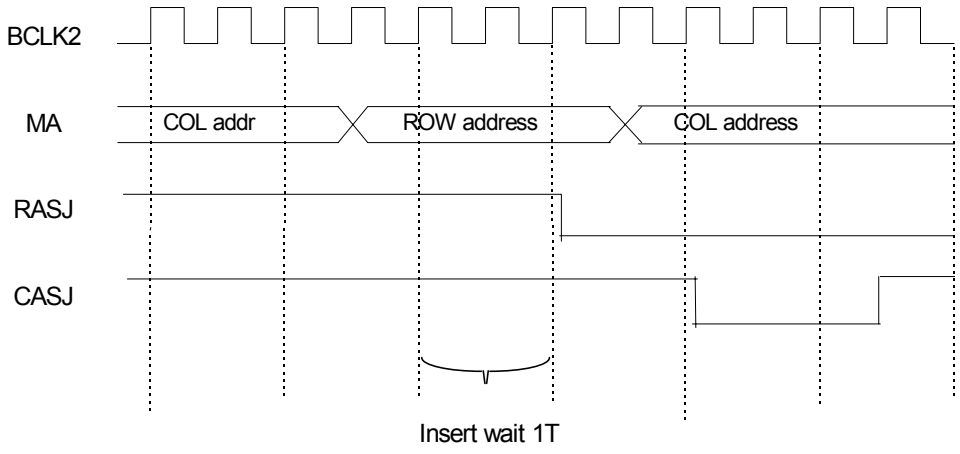
(c) CAS precharge time insert wait

Whatever memory read or write, it will insert 1T wait between the falling edges of both RASJ and CASJ, if D[4] of index 11h is set to high.



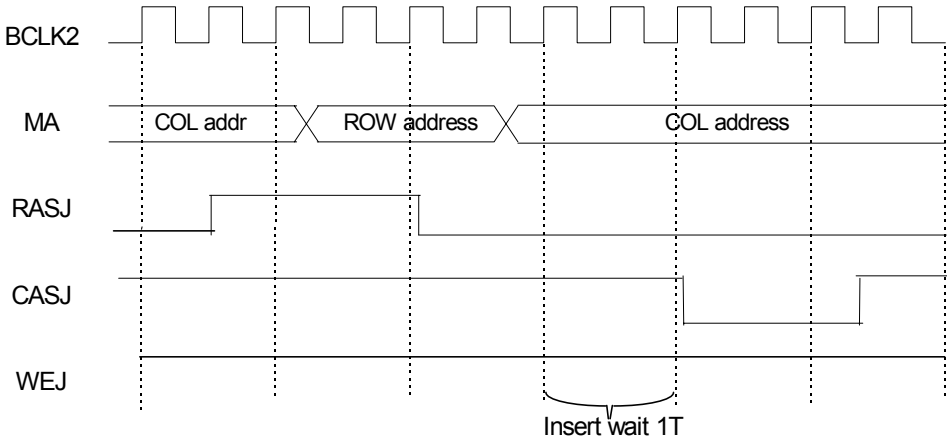
(d) RAS active time insert wait

If RAS is originally in miss state, that is RASJ = 1. We are able to prolong the inactive state of RAS for an extra 1T, before its falling edge, if D[3] of index 11h is set to high.



(e) Memory miss read RAS to CAS insert wait

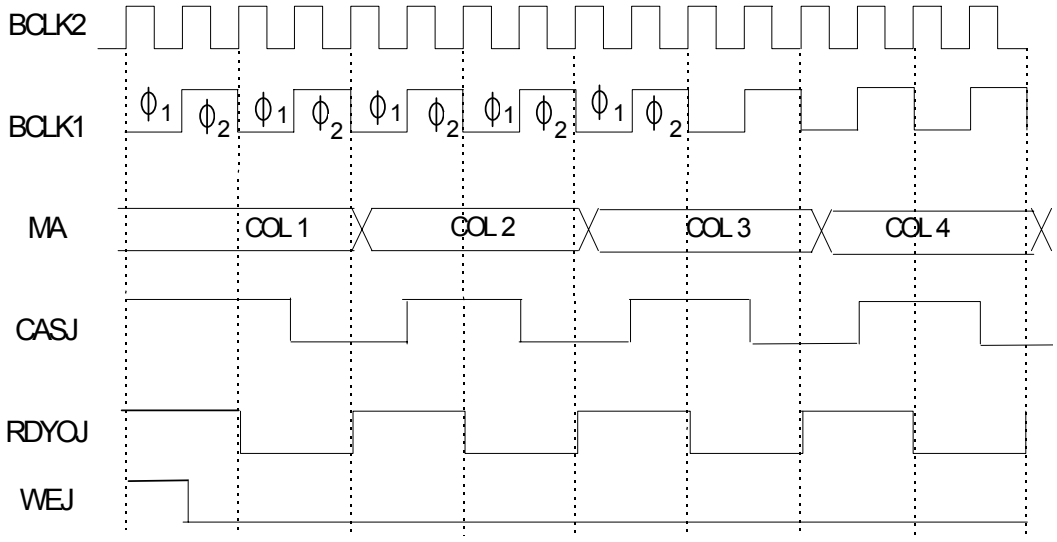
When memory read miss. We can add 1T wait between the falling edges of both RASJ and CASJ, if D[2] of index 12h is set to high.



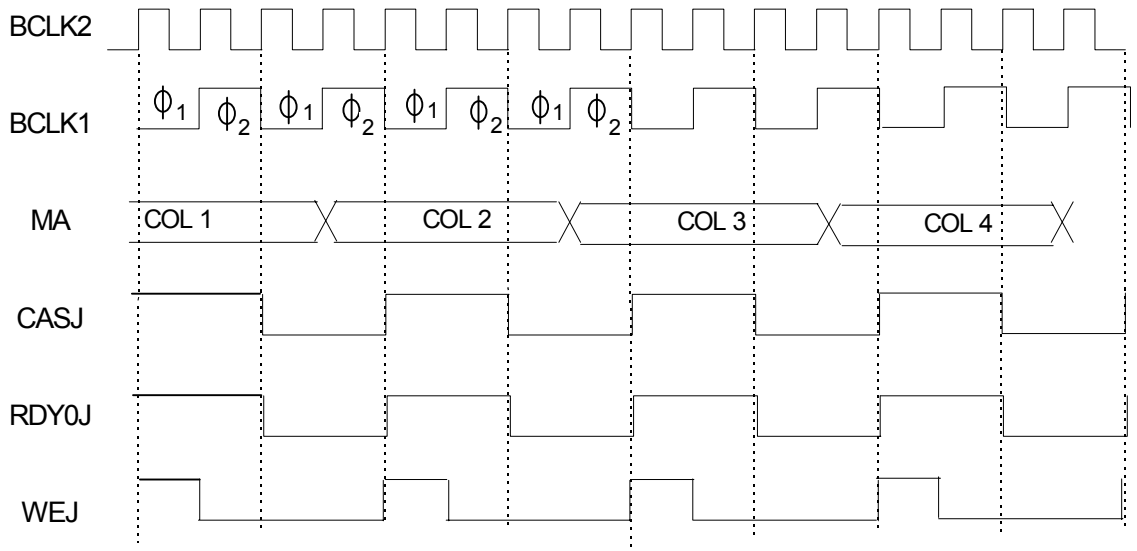
(f) Memory fast write hit insert wait

When memory write hits. This factor is capable of activating CASJ at phase 1 or phase 2 of BCLK2. If D[0] of index 12h is set to low, M6117D will activate CASJ at phase 2. In other words, the active CASJ will lag active RDYOJ by half T-cycle. That is early ready timing. If D[0] of index 12h is set to high, chip will activate CASJ at phase 1. So that active CASJ and RDY0J will be at the same phase.

(A) D[0] of index 12h is low



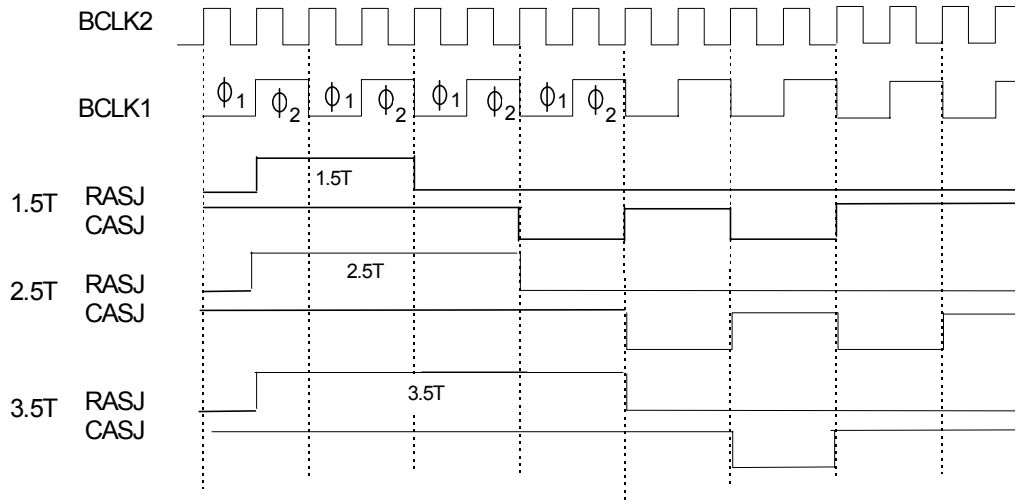
(B) D[0] of index 12h is high



(g) RAS precharge time insert wait

There are two bits to control RAS precharge timing, one is D[5] of index 11h, another is D[0] of the same index. Table as follows is the precharge time related to bit setting.

Index 11h : D[5]	D[0]	Pre-charge time
0	0	2.5T
0	1	1.5T
1	X	3.5T

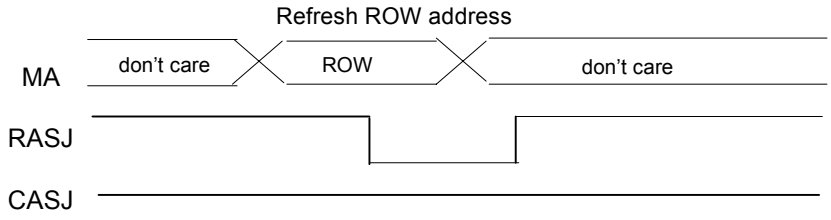


4.3.4 DRAM refreshing

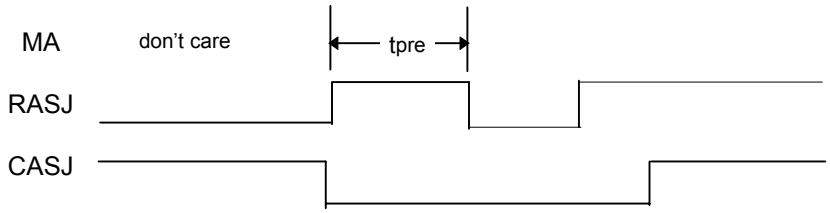
DRAM refresh cycle is 256 for every 4ms. However, for some DRAM products, the data at capacitance can be maintained more than 15 us. To get higher system performance, we can slow down refresh period for some DRAM products. By programming index 36h : D[5-4], we can get slow refresh period as follows:

Index 36h : D[5]	D[4]	Refresh period setting
0	0	15 us
0	1	120 us
1	0	15 us
1	1	60 us

We also support three types of DRAM refresh :
(A) RAS only refresh
This kind of refresh will be selected if D[1] of index 10h is set to '0' (low)



(B) CAS before RAS refresh
This kind of refresh will be selected if D[1] of index 10h is set to '1' (high)



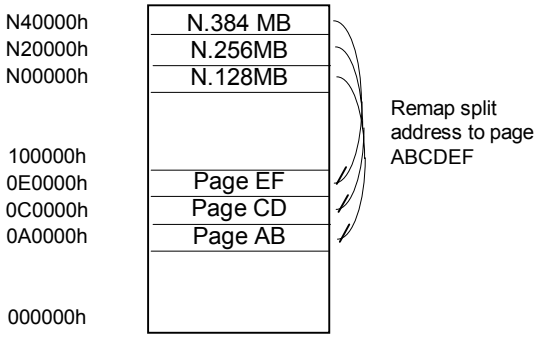
tpre : RAS precharge time

4.3.5 How to remap memory to top of memory

The address 0C0000h ~ 0FFFFFh is for ROM or reserved area. When this range of RAM is not used as shadow RAM, then the memory is wasted. However, we can use this area of RAM by remapping the higher address to the non-shadow RAM. In order to have continuous memory mapping, the remapping address selects the higher area to do so. For example, if we have 12MB DRAM on board, shadow RAM all disabled, then we can select 13MB (00D00000h) to be the address to remap. There are two remapping types determined by D[1] of index 11h, split (D[1]=0) and move-out (D[1]=1). By programming D[7-4] of index 12h, we can set the split address A23-A20. Memory split remapping can be disabled by programming index 11h : D[2] to 0. Please notice that index 11h : D[2] must be set to 1 and index 11h : D[1] must be set to 0 if you want to enable split remap. Otherwise, the move-out remap is selected when index 11h: D[1] is set to 1. Following are the different cases of memory remapping.

(A) No shadow, split address[23-20] = A[23-20], Remap type = split remap

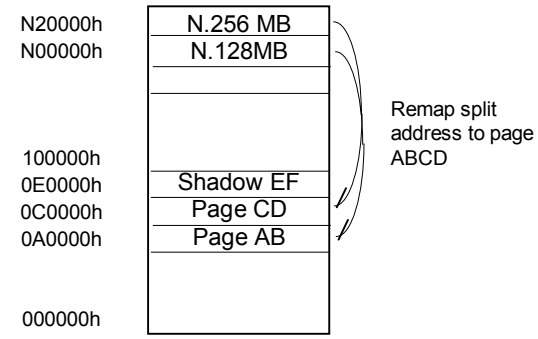
A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
0	0	0	x	0	0	0	0	1	0	1
0	0	1	x	0	0	0	0	1	1	0
0	1	0	x	0	0	0	0	1	1	1



where N < 0Fh

(B) Shadow Page EF, split address[23-20] = A[23-20], Remap type = split remap

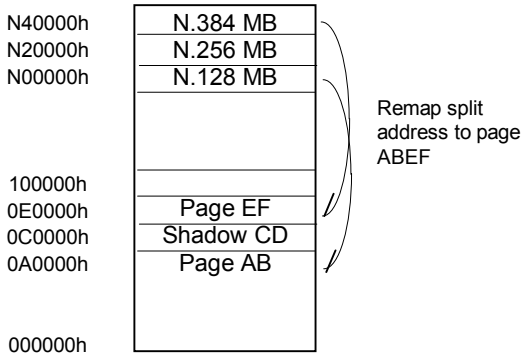
A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
0	0	0	x	0	0	0	0	1	0	1
0	0	1	x	0	0	0	0	1	1	0



where N < 0Fh

(C) Shadow Page CD, split address[23-20] = A[23-20], Remap type = split remap

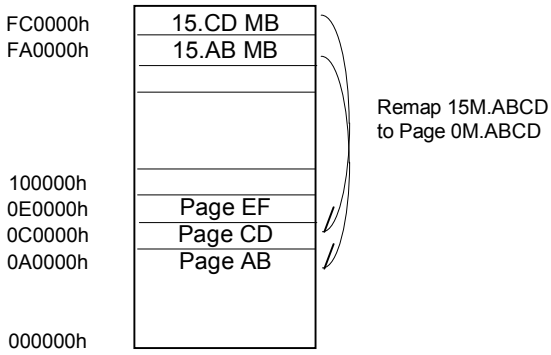
A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
0	0	0	x	0	0	0	0	1	0	1
0	1	0	x	0	0	0	0	1	1	1



where N < 0Fh

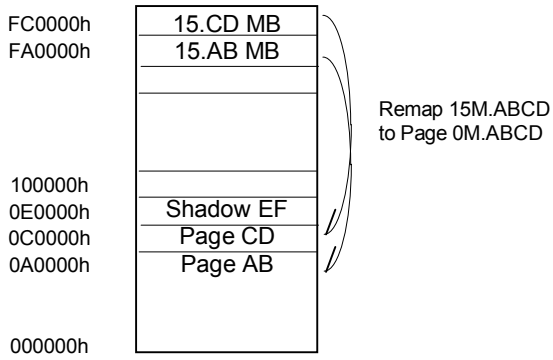
(D) No shadow, A[20-23]=1111, Remap type =Move-out remap and memory mode cannot be 10, 19, 21, 22, 25, 28, 29, 30, 31

A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
1	0	1	x	0	0	0	0	1	0	1
1	1	0	x	0	0	0	0	1	1	0



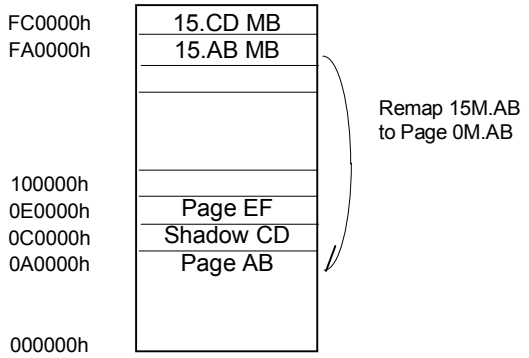
(E) Shadow EF, A[20-23] = 1111, Remap type=Move-out remap and memory mode cannot be 10, 19, 21, 22, 25, 28, 29, 30, 31

A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
1	0	1	x	0	0	0	0	1	0	1
1	1	0	x	0	0	0	0	1	1	0



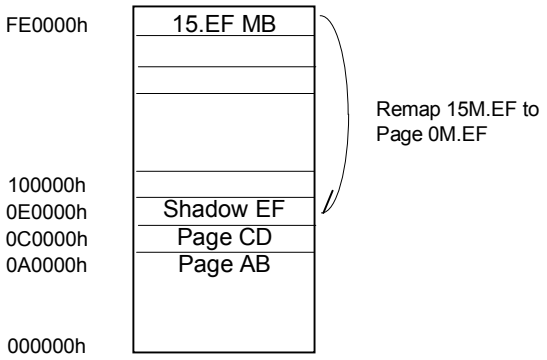
(F) Shadow CD, A[20-23]=1111, Remap type=Move-out remap and memory mode cannot be 10, 19, 21, 22, 25, 28, 29, 30, 31

A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
1	0	1	x	0	0	0	0	1	0	1



(G) Shadow EF, A[20-23]=1111, or A[20-23] = 0000, Remap type=Move-out remap and memory mode cannot be 10, 19, 21, 22, 25, 28, 29, 30, 31

A19	A18	A17	A16	PA23	PA22	PA21	PA20	PA19	PA18	PA17
1	1	1	x	0	0	0	0	1	1	1



4.3.6 Shadow Control

The address 0C0000h~ 0FFFFFh is for ROM or unused areas. When the range address is used for ROM, the system can use RAM to map the area to enhance performance. The address 0C0000~0FFFFFh is also called shadow region. The shadow region can be read/write control. For example, when it is read enable, write disable, the operation of shadow RAM is the same as ROM. By programming index 14h, 15h, BIOS programmer can set the read/write control function to initialize the system. Suppose 0C0000h~0C7FFFh video ROM is present, and 0C0000h~ 0C7FFFh region wants to be shadowed, then the setup steps are :

(1) Index 14h : D[1-0] = 00, Shadow region 0C0000h ~ 0C7FFFh read/write both disable. Allow the process to be read from ROM only.

(2) Index 14h : D[1-0] = 10, Shadow region 0C0000h ~ 0C7FFFh read disable, write enable. Allow the process to be read from ROM and write to DRAM (Shadow RAM). Then video ROM data copies to shadow RAM region.

(3) Index 14h : D[1-0] = 01, Shadow region 0C0000h ~0C7FFFh read enable, write disable. Allow the operation to be read from DRAM. The video ROM read process is via shadow RAM 0C0000h~ 0C7FFFh region, not via video ROM.

The range of 0C0000h ~ 0FFFFFh partitions to eight blocks, each block is 32KB. Each shadow region block can be shadow read/write disabled or enabled by programming index 14h, 15h.

The A0000h ~ B0000h region can set to shadow enable. If host read/write this region, the data will read/write from local memory when enable shadow.

How to set shadow A/B region ?
Index 3ch:
bit 3 = 0, Disable shadow A/B function
bit 3 = 1, Enable shadow A/B function
Index 12h:
bit 1 = 0, Disable shadow A/B region. All access to A/B memory region will pass to ISA
bit 1 = 1, Enable shadow A/B region. All access to A/B memory region will be at local memory.
Only both the index 3ch and 12h enable, the shadow A/B region will enable.

4.3.7 BIOS ROM control

The size of BIOS ROM can be 64KB or 128KB. When using 64KB BIOS ROM, then index 10h:D[0] sets to '0', and the address used can be 0F0000h~0FFFFFh or 0FF0000h ~ 0FFFFFFh. When 128KB BIOS ROM is used, index 10h : D[0] sets to '1' and the address used is 0E0000h~ 0FFFFFh. The BIOS ROM can be replaced by flash ROM to support ROM BIOS updatable by software program. Flash ROM is writable by activating write enable pin. Before writing data to flash ROM, we have to set index 20h : D[2] to '1'. Otherwise, flash ROM cannot accept it.

4.3.8 On board 15M~ 16M memory enable/disable control

On board 0F00000h~ 0FFFFFFh memory can be enabled/disabled by programming index 10h : D[2]. When D[2] =0, the on board 15M ~16M memory will be recognized as local memory. When D[2] =1, the on board 15M~16M range memory will not be recognized, and will be treated as ISA range.

4.4 ISA Bus Interface Control

The ISA bus controller and ISP devices are developed and verified by ALi's M1487/M1489 series.

4.4.1 ISA ATCLK frequency control

After powering-on, the default value of ISA ATCLK is 7.159 Mhz, this clock is changed by programming index 1Eh : D[2:0] to set to different frequencies to meet the system designer requirements.

Index 1Eh

D[2]	D[1]	D[0]	ATCLK
0	0	0	7.159 Mhz (def)
0	0	1	PCLK2/3
0	1	0	PCLK2/4 PCLK2/3
0	1	1	PCLK2/5
1	0	0	PCLK2/6
1	0	1	PCLK2/8
1	1	0	PCLK2/10
1	1	1	PCLK2/12

Note : PCLK2 means doubled CPU clock

To make sure the system boots normally, the default ATCLK is 7.159 Mhz. So system can boot at any CPU frequency. After powering on, BIOS can detect the CPU frequency, and set the desired AT clock frequency. For example, if CPU running at 40 Mhz, the PCLK2 will be 80 Mhz and if we choose D[2-0] = 110, this means ATCLK =PCLK2/10, then ATCLK is 8 MHz.
Note : The 82C54 has some limitations which require ISA ATCLK set as 7.159 MHz. Please refer to Appendix C.

4.4.2 I/O Recovery Control

For old slow ISA cards, I/O recovery time must be added to back ISA I/O commands. If an I/O writes too fast, the previous I/O write data will be overlaid by the later one, so the card will fail. The I/O recovery time recommends value of 500 ns and set by index 33h : D[7-4]. Notice that you have to enable the I/O recovery time in advance, otherwise index 33h : D[7-4] will not work. We separated on-chip decoded I/O port control and general purpose I/O port control to index 33h : D[2] and D[3] respectively.

8F-1,No.22,Wuchyuan 2RD.,Hsin Chuang city Taipei Hsien, Taiwan, R.O.C. Tel: 886-(02) 2298-0770 Fax: (02) 2299-1883

Index 33h

D[7-4]	I/O recovery time
0000	0 (default)
0001	250 ns
0010	500 ns
0011	750 ns
0100	1000 ns
0101	1250 ns
0110	1500 ns
0111	1750 ns
1000	2000 ns
1001	2250 ns
1010	2500 ns
1011	2750 ns
1100	3000 ns
1101	3250 ns
1110	3500 ns
1111	3750 ns

D[3]	I/O recovery
0	disable
1	enable

D[2]	On chip I/O recovery
0	disable
1	enable

4.4.3 ISA high speed change on fly

Since ISA bus is slow, our ISA high speed change-on-fly function permits ISA card operating in higher ATCLK during specific I/O or memory accessing cycles. Index 16h ~ 18h are used to define and mask ISA memory address set 1 which will fly to higher ATCLK frequency when setting addresses are matched. Index 19h~ 1Bh are used to define and mask ISA memory address set 2 which will fly to higher ATCLK frequency when setting addresses are matched. Index 1Ch~ 1Dh are used to define and mask ISA I/O address. For instance, if the CPU clock is 40 Mhz, PCLK2 = 80 Mhz and Index 1Eh : D[2:0] = 011, then the AT clock will be PCLK2/5 = 16 Mhz in normal speed address, and PCLK2/4 = 20 Mhz in high speed address.

High frequency	**Index 1Eh : D[2:0]**	**Normal frequency**
7.159 MHz	000	7.159 Mhz
PCLK2/2	001	PCLK2/3
PCLK2/3	010	PCLK2/4
PCLK2/4	011	PCLK2/5
PCLK2/5	100	PCLK2/6
PCLK2/6	101	PCLK2/8
PCLK2/8	110	PCLK2/10
PCLK2/10	111	PCLK2/12

Normal frequency goes to high frequency when address matches. High frequency goes back when address does not match.

4.5 Power Management

In M6117D internal circuit, it has an internal signal SMIJ which is used to inform system to enter Power Management (Hyper State Mode; HSM) space if an event happens. However, there are other extra choices to achieve power management. They are NMI, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, and IRQ15. Chip only switches the SMI signal to internal NMI or IRQs if it is selected when an event happens. Index 55h : D[1-0] and Index 38h : D[3-0] determine which one is selected. *Please refer to Appendix A and B for CPU information in this section.*

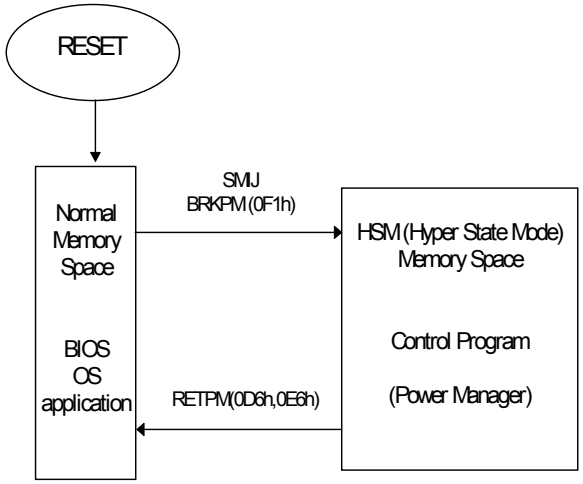
Index 55h

Index 55h : D[1-0]	Index 38h : D[3-0]	timing selection
00	xxxx	SMI timing support
01	xxxx	NMI timing support
10	xxxx	IRQ15 timing support
11	0011	IRQ3 timing support
11	0100	IRQ4 timing support
11	0101	IRQ5 timing support
11	0110	IRQ6 timing support
11	0111	IRQ7 timing support
11	1001	IRQ9 timing support
11	1010	IRQ10 timing support
11	1011	IRQ11 timing support
11	1100	IRQ12 timing support
11	1110	IRQ14 timing support
11	others	reserved

Notice that the system is not going to enter HSM space if you choose NMI or other IRQs timing support. All power management using NMI and other IRQs timing are handled by software.

4.5.1 SMI Structure

Like other green CPUs, M6117 needs a special memory space to place Hyper State Mode (HSM) routine if you would like to use M6117 deep green features. We can enter HSM space by hardware SMIJ (System Management Interrupt) or instruction BRKPM, OP code : 0F1h, and return by instruction RETPM, OP code: 0D6h, 0E6h. How to use power management functions efficiently to minimize the system power consumption is a challenge.



4.5.2 System Management Interrupt (SMI)

System management interrupt has the most priority to cause M6117D entering HSM space. Like non-maskable interrupt (NMI), M6117D will jump to SMI entry point or starting address, ROM area 0FFFFFF90h in default, after accepting SMI, this chip thus has entered HSM space. Depending on different applications, we can also change the page address of SMI entry point by way of updating the value of UGRS' which is a special 32-bit register in M6117 CPU core. For instance, if we write 0A0000h to UGRS before activating SMI, then M6117 will jump to 00AFF90h when SMI asserts. Following is a short sample of assembly code to implement the example above.

```
MOV EAX, 0A0000h
; LDUSR   UGRS, EAX
DB 0D6h, 0CAh, 03h, 0A0h
```

4.5.3 Enter and Exit the HSM(Hyper State Mode) space

If we select SMI to implement Power Management Mode, the CPU will switch memory space to HSM while an event happens. Also, we can use the instruction BRKPM(**opcode - DB 0F1h**) to enter HSM. The PV monitor interrupt (set by ***CR03h PMON***) and opcode trap(set by ***CR0Eh TOP*** and ***CR0Fh TCON***) can do the same operation.

The BRKPM (**opcode** - **DB 0F1h**) instruction or any equivalent interrupt transfers the values, which have been set before its generation with the registers indispensable in controlling the processor operation, to the high-order general purpose registers(shown below), and then switches the processor space to shift control to the specific physical addresses. Then CPU is brought to the following reset state:

16-bit context
Real Mode Addressing
Paging Off
Interrupt Disable

SMI, BRKPM instruction
PV monitor, and opcode trap

GR31	***CR00h***	- CR0
GR30	***EFLAGS***	
GR29	***AR1***	- CS-LIMIT
GR28	***SR1***	- CS-BASE
GR27	***EIP***	
GR26		
GR25		CS

EXP monitor

GR31	***CR00h***	- CR0
GR30	***EFLAGS***	
GR29	***AR1***	- CS-LIMIT
GR28	***SR1***	- CS-BASE
GR27	***EIP***	
GR26		EXT#
GR25		CS

The RETPM (**opcode** - **DB 0D6h 0E6h**) instruction causes the reverse operation of the BRKPM instruction. It returns control to the normal context. Note that save/restore is done only for ***CR00h***, ***AR1***, ***EFLAGS***, ***SR1***, ***EIP***, and ***CS*** for both **BRKPM** and **RETPM** instructions. Therefore, the contents of the other registers must be saved and restored by software.

When the original operating system is in protected mode and we enter HSM space, we need to handle the segment base and attribute registers carefully when the segment register is changed. Also, we can get other information from reading the ***GR31*** - ***GR25*** to do our application.

4.6 The way to generate system management interrupt

4.6.1 Mode timer time-out

There is a Mode timer in power management unit of M6117D, this is based on 14.318 Mhz frequency input. There are four time bases 1 sec, 10 secs, 1 min and 10 mins. The timer counter is from 0 to 15, so the combinations are as follows :

Time count	**Time base**			
	1 sec	10 sec	1 min	10 min
0	0 sec	0 sec	0 min	0 mins
1	1 sec	10 secs	1 min	10 mins
2	2 secs	20 secs	2 mins	20 mins
3	3 secs	30 secs	3 mins	30 mins
4	4 secs	40 secs	4 mins	40 mins
5	5 secs	50 secs	5 mins	50 mins
6	6 secs	60 secs	6 mins	60 mins
7	7 secs	70 secs	7 mins	70 mins
8	8 secs	80 secs	8 mins	80 mins
9	9 secs	90 secs	9 mins	90 mins
10	10 secs	100 secs	10 mins	100 mins
11	11 secs	110 secs	11 mins	110 mins
12	12 secs	120 secs	12 mins	120 mins
13	13 secs	130 secs	13 mins	130 mins
14	14 secs	140 secs	14 mins	140 mins
15	15 secs	150 secs	15 mins	150 mins

e.g. There are two possible settings for two minutes, (a) 10 secs time base, time count is 12.
(b) 1 minute time base, time count is 2.

The BIOS should choose the small time base to reduce time shift. In other words, small time base is more precise than bigger time base.

The configuration register index 64h is the timer setting.

Index 64h

D[7-4]	**Time count**
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

Index 64h

D[2]	Timer count/reset
0	Timer reset
1	Timer count

D[1-0]	Time base
0 0	1 second
0 1	10 seconds
1 0	1 minute
1 1	10 minutes

Once the mode timer counter is equal to the time count setting, then the time-out occurs. Time-out will generate a system management interrupt and index 5Bh will show 06h to manifest the interrupt cause. Notice that you should set index 59h : D[5] to '1' to activate mode timer even if you have already set the index 64h. We can prolong time delay for double of our time setting by programming index 69h : D[4] to '1' which is double counter time base control bit. When timer is enabled, any access to monitored device range, the corresponding timer will reset and restart counting until time-out is reached. For instance, mode timer will be reset when any key on keyboard is pressed for keyboard is the most possible monitored peripheral device.

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4.6.2 Interrupt request active

System will generate SMI as soon as any channel of 8259• IRQ happened if we have already programmed index 5Ch and 5Dh. System• definite instant SMI cause from it has the most priority among all interrupts. Moreover, index 57h:D[3] and index 5Ah :D[5] should be set to '1' to enable IRQ trigger SMI. Index 5Bh will show 08h after this SMI has occurred.

Index	5Ch	Index	5Dh
D[7]	IRQ7 selected	D[7]	IRQ15 selected
D[6]	IRQ6 selected	D[6]	IRQ14 selected
D[5]	IRQ5 selected	D[5]	IRQ13 selected
D[4]	IRQ4 selected	D[4]	IRQ12 selected
D[3]	IRQ3 selected	D[3]	IRQ11 selected
D[2]	NMI selected	D[2]	IRQ10 selected
D[1]	IRQ1 selected	D[1]	IRQ9 selected
D[0]	IRQ0 selected	D[0]	IRQ8 selected

The M6117D has 49 configuration registers, these registers reside at I/O port 23H (read/write), with index at output port 22H. Table 4-1 lists the internal registers summary. Section 4.2 describes the bit function of internal registers. Table 4-3 lists memory type configuration.

4.6.3 DMA channel request active

System will generate SMI as soon as any channel of 8237• DRQ happened if we have already programmed index 5Eh, besides index 57h :D[7] and index 5Ah : D[6] should be set to '1' to enable DRQ trigger SMI. Here, index 5Bh will show 09h after this SMI has occurred.

Index 5Eh	
D[7]	DRQ7 selected
D[6]	DRQ6 selected
D[5]	DRQ5 selected
D[4]	DRQ4 selected
D[3]	DRQ3 selected
D[2]	DRQ2 selected
D[1]	DRQ1 selected
D[0]	DRQ0 selected

4.6.4 IN access

IN access will happen when monitoring IRQ12, IRQ4, IRQ3 and IRQ1 (always enable) are asserting. Index 66h:D[7-5] is to define which IRQ channel is enabled as IN access, notice that IRQ1 is always enabled. SMI occurs when monitoring IN access is activating and then index 5Bh will show 0Ah.

Index 66h	
D[7]	IN monitor IRQ3 select
D[6]	IN monitor IRQ4 select
D[5]	IN monitor IRQ12 select

4.6.5 External switch

There are two external trigger signals to generate SMI, external SMI switch input (EXTSW2) and external suspend switch input (EXTSW1), both of them have the same function-trigger SMI. Index 58h :D[7-6] are the enable bits to EXTSW2 and EXTSW1 respectively. Each input trigger polarity can choose low-to-high active or high-to-low active or both depending on index 67h: D[1-0] respectively. These two input pins has internal debouncing circuit to prevent the miss action. But you can bypass internal debouncing circuit . Index 37H: D[5:4] are enable bits to bypass EXTSW2 and EXTSW1 internal debouncing circuit respectively. Index 5Bh will show 0Ch if SMI cause from EXTSW1 and 10h if SMI cause from EXTSW2.

4.6.6 Real Time Clock alarm

System will generate SMI when IRQ8 assert, if RTC has properly been programmed and the following control bits is set to '1' : index 57h :D[3], index 59h :D[6], index 5Ah :D[5] and index 5Dh:D[0]. Index 5Bh will show 0Dh after this event is asserted.

4.6.7 Software SMI

If index 56h :D[6] is set to '1' and D[7] of the same register is '1', system will generate SMI called software SMI. Index 5Bh will show 0Fh after this event.

4.6.8 VGA access

If index 57h:D[1] and index 5Ah:D[0] are set to '1', then system will generate SMI when memory write address matches 0A0000h~ 0B0000h with index 66h :D[0] is '1', or when I/O write address matches 3B0h~ 3BFh with index 66h :D[1] is '1'. Index 5Bh will show 11h after VGA access event.

4.6.9 Hard Disk Drive access

Hard disk drive operations will trigger SMI by programming following control bits to '1' = Index 57h :D[3], D[2] ; 5Ah:D[5], D[1] and 5Ch : D[5]. 12h will be shown on index 5Bh after HDD event.

4.6.10 Line Printer access

If indices 57h: D[4], D[3], 5Ah:D[5], D[2], and 5Ch:D[7] are set to '1', then it enables line printer access to activate SMI. Index 5Bh will show 13h to manifest SMI cause from line printer operation.

4.6.11 General purpose memory address access

If indices 6Ch, 6Dh, 6Eh, 6Fh were programmed in advance and control bits 58h:D[0], 5Ah:D[3], 6Bh :D[1] were set to '1' (enable), then system will generate SMI when memory read/write address matches the address defined in indices 6Ch~6Fh, called GP0 event. For example, If we write 10h to index 6Ch, 0Fh to index 6Dh, 00h to indices 6Eh and 6Fh, set index 58h: D[0], index 5Ah:D[3], index 6Bh: D[1] to high, then system will generate SMI when memory read/write address is the one during 1MB~2MB. Index 5Bh will show 14h after GP0 event.

4.6.12 General Purpose I/O address access

Similar to CP0 access, SMI will occur when I/O read/write address matches the address defined in index 70h, called GP1 event. In addition to programming 70h and 6Bh, index 58h: D[1], index 5Ah :D[4] and index 6Bh:D[0] should be set to '1', thus GP1 event will be enabled and index 5Bh will show 15h if any SMI occurs by GP1 event. Moreover, index 6Bh:D[7-4] offer three kinds of well defined I/O address group to cause GP1 event.

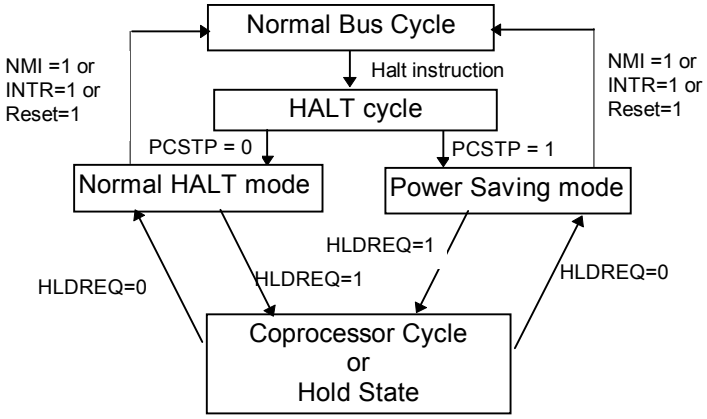
4.6.13 Special instruction to emulate SMI

Instruction BRKPM, OP code = 0F1h, will emulate M6117D entering HSM space as if SMI has occurred. This special instruction is only for emulation or testing, no programming is needed and of course index 5Bh will show nothing when designer uses BRKPM instruction.

4.7 How to enter power saving mode

M6117D can stop internal clock to its CPU core that will reduce almost 80% of its power consumption. Because our chip belongs to pure CMOS process, it will keep the internal states from leaking current when Vcc is still powered on and clock has stopped. There is one control bit, called as power clock stop (PCSTP), in internal control register to determine if M6117D is going to enter power saving mode or not. Here, we have a diagram to show the whole operation on accessing power saving mode. Notice that chip enters power saving mode by executing HALT instruction, and leave by any interrupt or reset.

M6117D Power Saving Mode



Question : How to set PCSTP ? (Power Clock Stop)
Answer : MOV EAX, 00008000h
DB 0D6h, 0FAh, 03h, 02h
/* MOV PWRCR, EA0 */

4.8 Speed LED flash control

System Designer can connect an LED to M6117D• CPUSPD pin to show LED flashing as a phenomenon in green mode. There are many varieties of LED flash combination including duty cycle, just program a value to index 71h. Then LED will start flashing.

Index	**71h**
D[4-2]	LED flash period
000	0.1 sec
001	0.2 sec
010	0.4 sec
011	0.8 sec
100	1.0 sec
101	2.0 sec
110	4.0 sec
111	8.0 sec

Index	71h
D[1-0]	LED duty cycle
00	disable
01	25%
10	50%
11	75%

4.9 General Purpose Output (GPO) and General Purpose Input (GPI)

M6117D support 16 independent GPOs and GPIs. This group of GPOs does not need external 74LS373 to latch as generate purpose output. Also this group of GPIs does not share with ISA data bus, so no external 74LS245 required.
Index 46h: Independent GPI[7-0] value. Default 00h Read only.
Index 47h: Independent GPO[7-0] value. Default 00h Read/Write.
Index 4Ch: Independent GPI[15-8]value. Default 00h Read only.
Index 4Dh: Independent GPO[15-8] value. Default 00h Read/Write.

M6117D supports another 16 expandable GPOs and 16 expandable GPIs. During normal condition, pins XD[7:0] are data bus to peripheral devices. But during cold reset, XD[7:0] is an input pin and latched by internal register - index 68h; the pin ENPOWER is also active at this time to latch XD[7:0] at external 74LS373. Because there is no default value in index 68h and as to XD[7:0] without any pulling resistor. Designer has to connect externally pull-up or pull down resistors to XD[7-0] to initialize index 68h. The index 68h : D[7-0] are both readable and writable. If BIOS wants to change the external 74LS373 latch value. It should first set index 68h :D[7:0] a new value, then write any value to index 73h, that will generate an ENPOWER signal to update 74LS373 latch value. The index value in 68h will appear at XD[7:0] bus and ENPOWER will update the XD value to 74LS373.
Index 3Dh: The high byte GPO value . Default 00h R/W
Index 3Eh: The low byte GPI value. Default 00h Read only.
Index 3Fh: The high byte GPI value. Default 00h Read only.

4.9.1 Generate GPOs method
(1) Use external 2 X 74373 input connect to SD bus. The latch enable pin connects to ENPOWER.
(2) Set index 68h and 3Dh to desired GPO value.
(3) Write index 73h.
(4) Then data stored in index 68h will be sent to SD[7:0] and XD[7:0]. Data stored in Index 3Dh will be sent to SD[15:8] and ENPOWER will be active.
(5) The value will be latched by 74373.

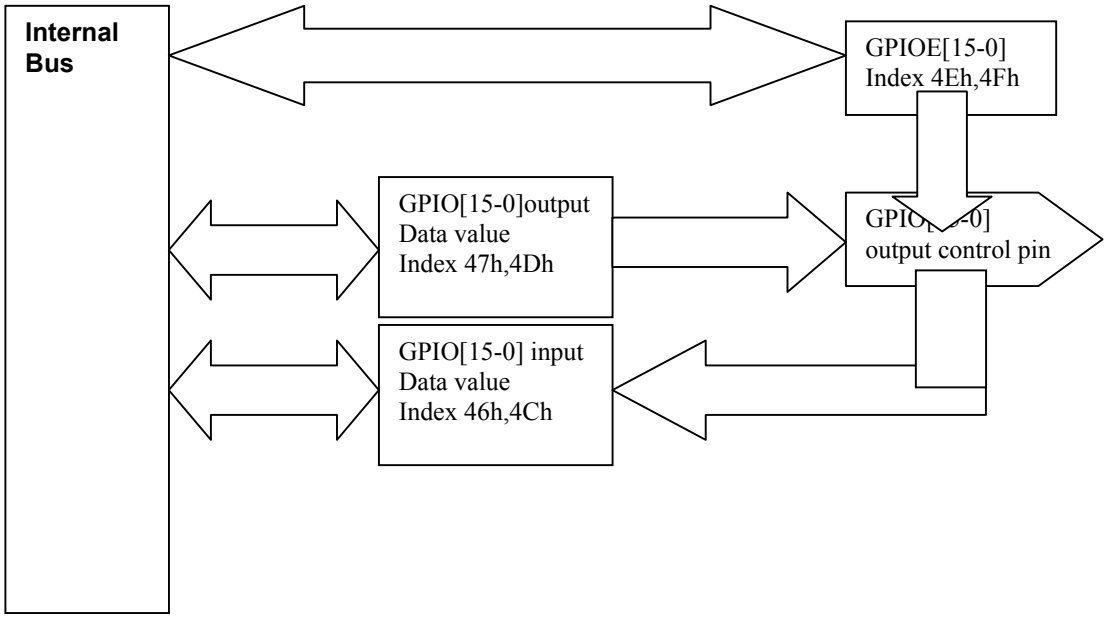
4.9.2 Generate GPIs method
(1) Add external 2 X 74245, the input connects to GPIs, the output connects to ISA SD bus. The OE control connects to ISA REFRESHJ.
(2) When REFRESHJ is active, the SD will become input and M6117D will use MEMRJ rising edge to latch the SD value.
(3) Every 15us, the GPIs value will be updated.
(4) BIOS can read the GPI• value through index 3Fh which store SD[15:0] value.

4.9.3 Generate Independent GPIOs as GPO method
(1) Write the desired value to index 47H , 4DH.
(2) Choose any GPIO as GPO by program GPIOE index 4EH , 4FH , and desired value will appear on independent GPO pins right away.

4.9.4 Generate Independent GPIOs as GPI method
(1) The M6117D will use IOR 46H , 4CH rising edge to latch the independent GPI value.

(2) BIOS can read the GPI value through index 46H and 4CH which store independent GPI value.

4.9.5 GPIOs block diagram



4.10 Watchdog timer

The watchdog timer uses 32.768 kHz frequency source to count a 24-bit counter so the time range is from 30.5u sec to 512 sec with resolution 30.5u sec. When timer times out, a system reset, NMI or IRQ may happen to be decided by BIOS programming. Please refer to see Appendix.

4.10.1 How to set the watchdog timer function ?

Index 37h :
Bit 6 = 0, Disable watchdog timer
Bit 6 = 1, Enable watchdog timer
Bit 7 = 0, Counter read mode. When read from index 3Bh, 3Ah, 39h, the return value is the setting counter value
Bit 7 = 1, Counter read mode. When bit 7 set from 0 to 1, the counter present value will be latched to buffer. When read from 3Bh, 3Ah, 39h, the return value is the buffer value. The counter will keep on counting.
Index 3Ch:
Bit 7 = 0, Read only, Watchdog timer time out event does not happen.
Bit 7 = 1, Read only, Watchdog timer time out event happens.

Index 3Bh, 3Ah, 39h : Counter

	3Bh	3Ah	39h
	D7……D0	D7……D0	D7……D0
Counter	Most SBit ……•east SBit		

4.10.2 How to set the watchdog timer counter ?

(1) Set Bit 6 = 0 to disable the timer
(2) Write the desired counter value to 3Bh, 3Ah, 39h.
(3) Set Bit 6 = 1 to enable the timer, the counter will begin to count up.
(4) When counter reaches the setting value, the time out will generate signal setting by index 38h bit[7:4]
(5) BIOS can read index 3Ch Bit 7 to decide whether the Watchdog timeout event will happen or not.

Index 38h : Bit[7:4] : time out generate signal select

Index 38h D[7:4]	timeout generate signal
0000	Reserved
0001	IRQ3
0010	IRQ4
0011	IRQ5
0100	IRQ6
0101	IRQ7
0110	IRQ9
0111	IRQ10
1000	IRQ11
1001	IRQ12
1010	IRQ14
1011	IRQ15
1100	NMI
1101	System reset
1110	Reserved
1111	Reserved

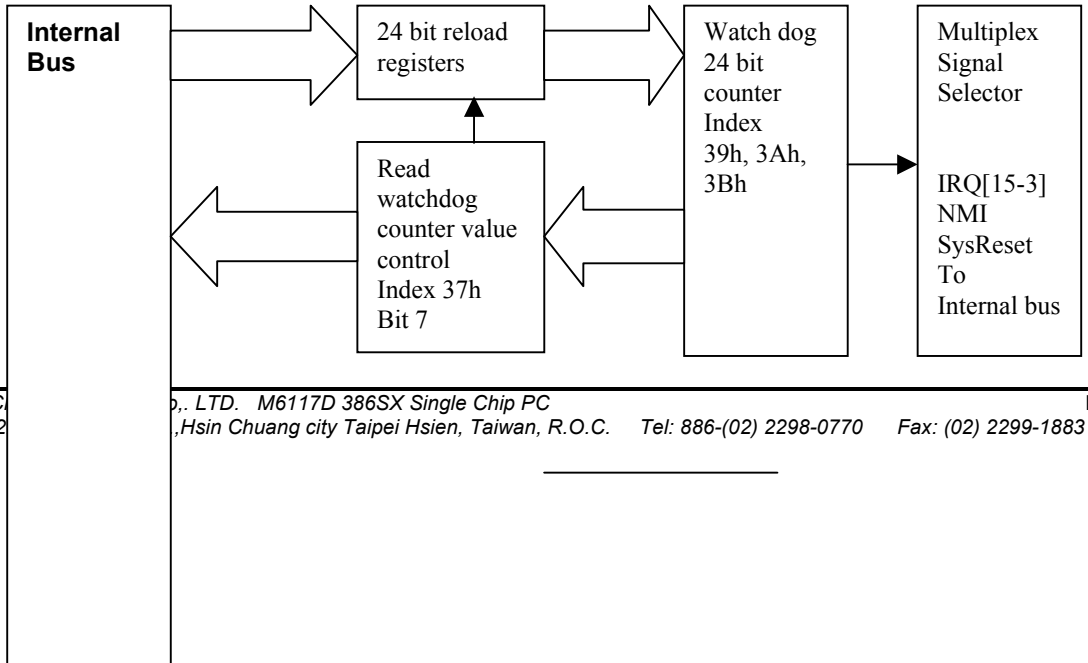
4.10.3 How to read the watchdog timer counter value when its counting ?

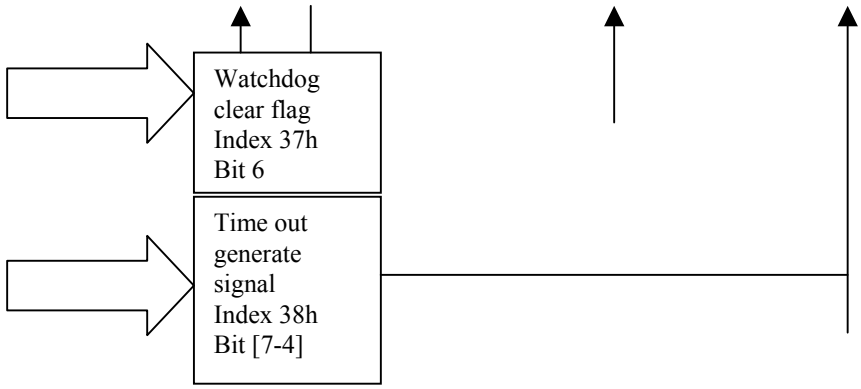
(1) Set Bit 7 = 1 to latch value
(2) Read the value in register index 3Bh,3Ah,39h. Then this is the on going value of counter.

4.10.4 How to clear the watchdog timer counter ?

(1) Set Bit 6 = 0 to disable timer. This will also clear counter at the same time.

4.10.4 Watchdog timer block diagram





4.11 IDE interface

How to select IDE interface ?

Write index 3Ch bit[0] to select IDE channel as primary or secondary.

Index 3Ch : D[0]	D [0] = 0	D[0] = 1
Channel	Primary	Secondary
HDCS0J	1F0 - 1F7	170 - 177
HDCS1J	3F6	376

4.12 General Purpose Chip Select

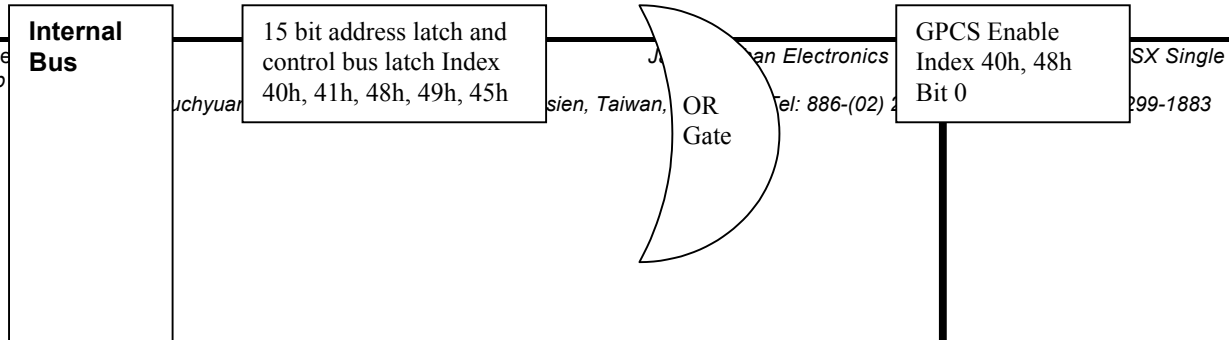
M6117D define two general purpose chip select output pin with programmable address and range of memory and I/O access. In addition to that, it also can be programmed as actived by either memory or I/O read / write command.

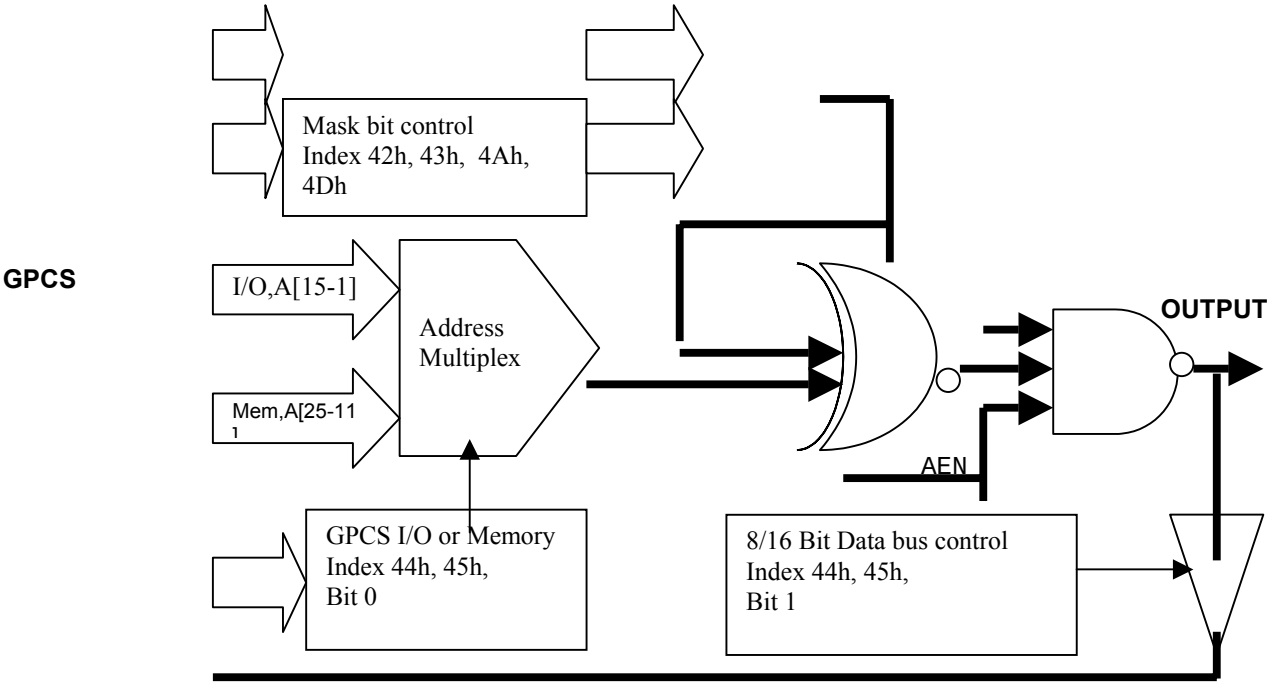
4.12.1 How to setting General Purpose Chip Select ?

(1) Set Index 44h : D[0] to decide GPCS0J represent memory or I/O access.
(2) Set Index 41h : D[7~0] and Index 40h : D[7~1] to decide starting address A[25-11] or A[15-1] depend on memory or I/O, respectively.
(3) Set Index 43h : D[7~0] and Index 42h : D[7~1] to decide the address range by mask A[25-11] or A[15-1] depend on memory or I/O, respectively. E.g. for memory case, mask A[11] will cause no comparison of A[11], which means the decode cover 4K byte memory range started from starting address defined in step (2).
(4) Set Index 40h : D[0] = 1 to enable GPCS0J. If GPCS0J represent address decode only, then the procedure is finished.
(5) If GPCS0J need to "filter" out read or write command, then Index 44h : D[5~2] can be used to select read or write command to qualify decode. I.e. for memory access case, set Index 44h : D[2] = 1 cause GPCS0J active only happen when I/O read cycle. This is typical case to protect device from incorrectly write data in.

Please refer to see Appendix.

4.12.1 How to setting General Purpose Chip Select ?





4.12 Register Summary

Port	Index	Attribute	Register
22H		R/W	Index register.
23H	10H	R/W	ROM size, refresh type and DRAM mode setting.
23H	11H	R/W	Memory Controller function setting.
23H	12H	R/W	Split address and miscellaneous function
23H	13H	R/W	Lock register
23H	14H	R/W	Page CD shadow area setting
23H	15H	R/W	Page EF shadow area setting
23H	16H	R/W	ISA high speed memory range setting (group 1)
23H	17H	R/W	ISA high speed memory range setting (group 1)
23H	18H	R/W	ISA high speed memory range setting (group 1)
23H	19H	R/W	ISA high speed memory range setting (group 2)
23H	1AH	R/W	ISA high speed memory range setting (group 2)
23H	1BH	R/W	ISA high speed memory range setting (group 2)
23H	1CH	R/W	ISA high speed I/O range setting (group 1)
23H	1DH	R/W	ISA high speed I/O range setting (group 1)
23H	1EH	R/W	ISA AT Clock Definition
23H	20H	R/W	Address remap setting in Power saving mode
23H	30H	R	Clock speed status
23H	31H	R/W	Fast RC and Gate A20 setting
23H	32H	R/W	ISA high speed switching
23H	33H	R/W	I/O recovery setting

23H	34H	Read Only	Hardware power-on configuration port
23H	35H	Read Only	Hardware power-on configuration port
23H	36H	R/W	Chip version and miscellaneous function
23H	37H	R/W	Watchdog timer / external switch / mouse / IDE / EDO DRAM function enable
23H	38H	R/W	Watchdog time out report signal select / SMI relocate select
23H	39H	R/W	Watchdog timer counter value (byte 0)
23H	3AH	R/W	Watchdog timer counter value (byte 1)
23H	3BH	R/W	Watchdog timer counter value (byte 2)
23H	3CH	R/W	Watchdog time out dispatch / Memory shadow AB / IRQ level / EDO timing detect / IDE channel function selection
23H	3DH	R/W	GPO high byte storage register
23H	3EH	Read Only	GPI low byte storage register
23H	3FH	Read Only	GPI high byte storage register
23H	40H	R/W	Chip select 0 channel address A[7-1]
23H	41H	R/W	Chip select 0 channel address A[15-8]
23H	42H	R/W	Chip select 0 channel mask address MSA[7-1]
23H	43H	R/W	Chip select 0 channel mask address MSA[15-8]
23H	44H	R/W	Configure general purpose chip select
23H	45H	R/W	Configure general purpose chip select
23H	46H	Read Only	Independent GPI [7:0] storage register
23H	47H	R/W	Independent GPO[7:0] storage register
23H	48H	R/W	Chip select 1channel address A[7:1]
23H	49H	R/W	Chip select 1channel address A[15:8]
23H	4AH	R/W	Chip select 1 channel mask address MSA[7-1]
23H	4BH	R/W	Chip select 1 channel mask address MSA[15-8]
23H	4CH	Read Only	Independent GPI [15:8] storage register
23H	4DH	R/W	Independent GPO[15:8] storage register
23H	4EH	R/W	Independent GPIOE[7:0]
23H	4FH	R/W	Independent GPIOE[15:8]
23H	55H	R/W	Power Management Unit Configuration port (First)
23H	56H	R/W	Power Management Unit Configuration port (Second)
23H	57H	R/W	Mode Select of combination of Idle detection
23H	58H	R/W	Generating SMI source selecting
23H	59H	R/W	Timer time-out selection
23H	5AH	R/W	Peripheral access selection
23H	5BH	R/W	SMIJ cause setting
23H	5CH	R/W	IRQ event channel selected control (First)
23H	5DH	R/W	IRQ event channel selected control (Second)
23H	5EH	R/W	DRQ event channel selected control

Table 4-10 Configuration registers (continued)

Port	Index	Attribute	Register
23H	64H	R/W	Mode timer setting
23H	66H	R/W	VGA and IN monitor setting
23H	67H	R/W	EXTSW1/EXTSW2 input polarity select
23H	68H	R/W	Power on latched power control initial status
23H	69H	R/W	Timer counter status setting
23H	6AH	Read Only	DOZE, STANDBY and SUSPEND timer time-out status
23H	6BH	R/W	GP1 address function
23H	6CH	R/W	Define GP0 memory address A[23-16]
23H	6DH	R/W	Define GP0 memory address A[23-16] mask bits
23H	6EH	R/W	Define GP0 memory address A[25-24]
23H	6FH	R/W	Define GP0 memory address A[25-24] mask bits

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23H	70H	R/W	Define GP1 I/O port address SA[9-2]
23H	71H	R/W	Mode LED function
23H	72H	R/W	Shadow I/O port for the data of port 70H
23H	73H	Write Only	Power control status output command.

4.13 Register Bit Definition

The details of M6117D configuration registers are described as follows :

PORT 22H default 00H

Bit	Description
7~0	Index of Configuration register

PORT 23H default 00H

Bit	Description
7~0	Data of Configuration register if unlock register unlocked.

INDEX 10H default 00H

Bit	Description
7~3	The five bits are used to set the memory type, the DRAM type is described in memory type table. D[7-4]=PM[3-0] & D3=PM4
2	The on board memory 15M ~ 16M-1 0 : enable 1 : disable
1	Two different refresh types: RAS only or CAS before RAS refresh. 0 : RAS only refresh 1 : CAS before RAS refresh
0	0 : 64KB ROM/EPROM (0F0000~ 0FFFFF/ FF0000~FFFFFF) 1 : 128K ROM/EPROM (0E0000~ 0FFFFF/ FE0000~FFFFFF)

INDEX 11H default F8H

Bit	Description
7	Memory write access time insert wait (BWAIT) 0 : disable 1 : enable
6	Memory CAS read access time insert wait (CASLWT) 0 : disable 1 : enable
5	Slow RAS precharge time 0 : see bit 0 below 1 : 3.5T
4	CAS precharge time insert wait for RAS to CAS delay (CASHWT) 0 : disable 1 : enable
3	RAS active time insert wait (RWAIT) 0 : disable 1 : enable
2	Memory remap 0 : disable 1 : enable
1	Select re-map mode 0 : split 1 : move-out
0	Fast RAS pre-charge time 0 : 2.5T 1 : 1.5T

INDEX 12H default 10H

Bit	Description
7~4	Split address SP[23-20]
3	reserved
2	Memory read miss RAS to CAS insert wait (MCASHWT) 0 : disable 1 : enable
1	Shadow RAM 0A0000h~0BFFFFh read/write control 0 : disable 1 : enable
0	Memory fast write hit insert phase (FSTWTHIT) 0 : PH2 1 : PH1

INDEX 13H default 00H

Bit	Description
7-0	C5h : Unlock configuration Register 00h : Lock Configuration Register

INDEX 14H default 00H

Bit	Description
7	Shadow RAM 0D8000~0DFFFF write 0 : disable 1 : enable
6	Shadow RAM 0D8000~0DFFFF read 0 : disable 1 : enable
5	Shadow RAM 0D0000~0D7FFF write 0 : disable 1 : enable
4	Shadow RAM 0D0000~0D7FFF read 0 : disable 1 : enable
3	Shadow RAM 0C8000~0CFFFF write 0 : disable 1 : enable
2	Shadow RAM 0C8000~0CFFFF read 0 : disable 1 : enable
1	Shadow RAM 0C0000~0C7FFF write 0 : disable 1 : enable
0	Shadow RAM 0C0000~0C7FFF read 0 : disable 1 : enable

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INDEX 15H default 00H

Bit	Description
7	Shadow RAM 0F8000~0FFFFF write 0 : disable 1 : enable
6	Shadow RAM 0F8000~0FFFFF read 0 : disable 1 : enable
5	Shadow RAM 0F0000~0F7FFF write 0 : disable 1 : enable
4	Shadow RAM 0F0000~0F7FFF read 0 : disable 1 : enable
3	Shadow RAM 0E8000~0EFFFF write 0 : disable 1 : enable
2	Shadow RAM 0E8000~0EFFFF read 0 : disable 1 : enable
1	Shadow RAM 0E0000~0E7FFF write 0 : disable 1 : enable
0	Shadow RAM 0E0000~0E7FFF read 0 : disable 1 : enable

INDEX 16H default 00H

Bit	Description
7~4	ISA high speed memory address A[23-20] set 1
3~0	ISA high speed memory address A[19-16] set 1

INDEX 17H default FFH

Bit	Description
7~4	ISA high speed memory address mask A[23-20] set 1
3~0	ISA high speed memory address mask A[19-16] set 1

INDEX 18H default F0H

Bit	Description
7~4	ISA high speed memory address mask A[15-12] set 1
3~0	ISA high speed memory address A[15-12] set 1

INDEX 19H default 00H

Bit	Description
7~4	ISA high speed memory address A[23-20] set 2
3~0	ISA high speed memory address A[19-16] set 2

INDEX 1AH default FFH

Bit	Description
7~4	ISA high speed memory address mask A[23-20] set 2
3~0	ISA high speed memory address mask* A[19-16] set 2

INDEX 1BH default F0H

Bit	Description
7~4	ISA high speed memory address mask* A[15-12] set 2
3~0	ISA high speed memory address A[15-12] set 2

INDEX 1CH default 00H

Bit	Description
7~4	ISA high speed I/O address A[9-6]
3~0	ISA high speed I/O address A[5-2]

INDEX 1DH default FFH

Bit	Description
7~4	ISA high speed I/O address mask* A[9-6]
3~0	ISA high speed I/O address mask* A[5-2]

** Mask Bit = 1 : Compare this address bit.*
0 : Do not compare this address.

INDEX 1EH default 00H

Bit	Description
7~3	reserved
2~0	ATCLK1 Definition

High Freq.	ATCLK[2:0]	Normal Freq.
14.318/2	0 0 0	14.318/2
PCLK2/2	0 0 1	PCLK2/3
PCLK2/3	0 1 0	PCLK2/4
PCLK2/4	0 1 1	PCLK2/5
PCLK2/5	1 0 0	PCLK2/6
PCLK2/6	1 0 1	PCLK2/8
PCLK2/8	1 1 0	PCLK2/10
PCLK2/10	1 1 1	PCLK2/12

INDEX 20H default 80H

Bit	Description
7	DRAM controller 0 : disable 1 : enable
6	reserved
5~4	Allocation remapping when SMI occurs, D3 must be enabled except remapping to ROM area 0 0 : Remap to ROM area 0 1 : Remap to page A,B 1 0 : Remap to page E 1 1 : Remap to page F
3	Remap SMI routine to local memory when this bit is set to high
2	Write to Flash ROM 0 : disable 1 : enable
1	DRAM self refresh (Index 10h D[1] must be 1) 0 : disable 1 : enable
0	Force ROM area remapping, disable remapping SMI routine to A, B page in local memory when this bit is set to high.

INDEX 30H default 08H

Bit	Description
7~4	reserved, must be 0
3	CPU speed, read only. 0 : low 1 : high
2~0	reserved, must be 0

INDEX 31H default 01H

Bit	Description
7~6	reserved
5	Fast reset state 0 : enable 1 : disable
4	reserved
3 ~ 1	reserved, must be 0
0	Fast gate A20 0 : disable 1 : enable

INDEX 32H default 00H

Bit	Description
7	ISA I/O high speed 0 : disable 1 : enable
6	ISA memory high speed 0 : disable 1 : enable
5~1	reserved, must be 0.
0	Port F1 reset NP 0 : disable 1 : enable

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INDEX 33H default 00H

Bit	Description
7~4	I/O recovery period definition (unit : 250ns)
3	I/O recovery 0 : disable 1 : enable
2	On-chip I/O recovery 0 : disable 1 : enable
1	reserved
0	Must be 0

INDEX 34H (Power-on setup, Read only)

Bit	No., Name	Description
7~6		reserved
5	26, DACK6J	reserved, must be pulled high
4	199, AEN	ISA clock test mode, when TESTJ = 0
3	22, DACK3J	reserved, must be pulled high bit is reversed when readout
2	20, DACK2J	Internal RTC 0 : disable 1 : enable
1		Reserved
0	16, DACK0J	reserved, must be pulled low. Read 0=C mode, 1=D mode.

INDEX 35H (Power-on setup, Read only)

Bit	No., Name	Description
7	119, ROMKBCSJ	reserved, must be pulled low.
6	24, DACK5J	reserved, must be pulled low.
5	28, DACK7J	Internal Keyboard Controller selection 0 : disable 1 : enable
4~2		reserved, must be 0.
1	18, DACK1J	Memory parity check 0 : disable 1 : enable
0		reserved

INDEX 36H default 00H

Bit	Description
7	16 bit ISA cycle insert 1 wait 0 : disable 1 : enable
6	PS/2 mouse IRQ12 timing 0 : direct connect IRQ12 to 8259 1 : send IRQ12 to 8259 after latch
5~4	Slow refresh control bits : Refresh period 0 0 : 15 us 0 1 : 120 us 1 0 : 15 us 1 1 : 60 us
3	reserved, must be 0
2~0	Chip version (Read only) 010 : M6117D

INDEX 37H default 00H

Bit	Description
7	Latch Watchdog timer value and counter read mode. 0: When read from Index3BH,3AH,39H, the read value is the setting counter value 1: When bit 7 set from 0 to 1, the counter present value will be latched to buffer. When read from Index 3BH,3AH,39H, the read value is the buffer value. The counter will keep on counting.
6	Watchdog timer 0: disable 1: enable
5	EXTSW2 de-bouncing circuit 0: enable internal de-bouncing circuit 1: bypass internal de-bouncing circuit
4	EXTSW1 de-bouncing circuit 0: enable internal de-bouncing circuit 1: bypass internal de-bouncing circuit
3	Reserved, must be 0
2	Internal mouse selection 0: disable 1: enable
1	Reserved, must be low
0	EDO DRAM mode 0: disable 1: enable

INDEX 38H default 00H

Bit	Description
7~4	Watchdog timer time out report signal select 0000: Reserved 0001: IRQ3 selected 0010: IRQ4 selected 0011: IRQ5 selected 0100: IRQ6 selected 0101: IRQ7 selected 0110: IRQ9 selected 0111: IRQ10 selected 1000: IRQ11 selected 1001: IRQ12 selected 1010: IRQ14 selected 1011: IRQ15 selected 1100: NMI selected 1101: system reset selected 1110: Reserved 1111: Reserved
3~0	SMI relocate to IRQ 0000: depend on Index 55H setting 0001: Reserved 0010: Reserved 0011: IRQ3 timing support 0100: IRQ4 timing support 0101: IRQ5 timing support 0110: IRQ6 timing support 0111: IRQ7 timing support 1000: Reserved 1001: IRQ9 timing support 1010: IRQ10 timing support 1011: IRQ11 timing support 1100: IRQ12 timing support 1101: Reserved 1110: IRQ14 timing support 1111: Reserved

INDEX 39H default 00H

Bit	Description
7~0	Watchdog timer counter value, byte 0

INDEX 3AH default 00H

Bit	Description
7~0	Watchdog timer counter value, byte 1

INDEX 3BH default 00H

Bit	Description
7~0	Watchdog timer counter value, byte 2

	3Bh	3Ah	39h
	D7……D0	D7……D0	D7……D0
Counter	Most SBit ……•east SBit		

INDEX 3CH	default 00H
Bit	Description
7	Watchdog timer time out 0: not happened 1: happened
6	Reserved
5	Reserved
4	Reserved
3	Memory Shadow A, B page function 0: disable 1: enable
2	IRQ Level trigger selection. 0: negative level trigger 1: level trigger
1	EDO DRAM timing detect mode 0: disable 1: enable
0	IDE channel selection 0: primary channel selected 1: secondary channel selected

INDEX 3DH	default 00H
Bit	Description
7~0	GPO signals. When write index 73H, Bit 7~0 will sent to SD[15:8]

INDEX 3EH	default 00H
Bit	Description
7~0	GPI signals. When REFRESHJ is active, the SD will become input and M6117D will use MEMRJ rising edge to latch the SD[7:0] to Bit 7~0. Read only

INDEX 3FH	default 00H
Bit	Description
7~0	When REFRESHJ is active, the SD will become input and M6117D will use MEMRJ rising edge to latch the SD[16:8] to Bit 7~0. Read only.

INDEX 40H	default 00H
Bit	Description
7~1	Chip select 0 channel address A[7-1].
0	1: GPCS0J enable 0: GPCS0J disable

INDEX 41H	default 00H
Bit	Description
7~0	Chip select 0 channel address A[15-8].

INDEX 42H	default 00H
Bit	Description
7~1	Chip select 0 channel mask address MSA[7-1]. 0=compare, 1= don't care.
0	1: PS2 IRQ1 timing enable 0: disable

INDEX 43H	default 00H
Bit	Description
7~0	Chip select 0 channel mask address MSA[15-8]. 0=compare, 1= don't care.

NDEX 44H	default 00H
Bit	Description
7~6	Reserved
5	GPCS0J qualify with ISA MEMR. 1:enable 0:disable
4	GPCS0J qualify with ISA MEMW 1:enable 0:disable
3	GPCS0J qualify with ISA IOR. 1:enable 0:disable
2	GPCS0J qualify with ISA IOW. 1:enable 0:disable
1	Configure channel 0 16/8 bits 1:enable 16 bits 0:enable 8 bits
0	Configure channel 0 address 1:enable memory address A[25-11] 0:enable IO address A[15-1]

NDEX 45H	default 00H
Bit	Description
7~6	Reserved
5	GPCS1J qualify with ISA MEMR. 1:enable 0:disable
4	GPCS1J qualify with ISA MEMW 1:enable 0:disable
3	GPCS1J qualify with ISA IOR. 1:enable 0:disable
2	GPCS1J qualify with ISA IOW. 1:enable 0:disable
1	Configure channel 1 16/8 bits 1:enable 16 bits 0:enable 8 bits
0	Configure channel 1 address 1:enable memory address A[25-11] 0:enable IO address A[15-1]

NDEX 46H	default 00H
Bit	Description
7~0	When IOR Index 46H is active, the independent GPIO[7-0] will be latch to bit GPI[7-0] . This is Read Only.

NDEX 47H default 00H

Bit	Description
7~0	Independent GPIO[7-0] signal output and storage register. When write value to this register, bit7~0 will be sent out to GPO[7-0] pins.

INDEX 48H default 00H

Bit	Description
7~1	Chip select 1 channel address A[7-1].
0	1: GPCS1J enable 0: GPCS1J disable

INDEX 49H default 00H

Bit	Description
7~0	Chip select 1 channel address A[15-8].

INDEX 4AH default 00H

Bit	Description
7~1	Chip select 1 channel mask address MSA[7-1]. 0=compare, 1= don't care.
0	Reserved

INDEX 4BH default 00H

Bit	Description
7~0	Chip select 1 channel mask address MSA[15-8]. 0=compare, 1= don't care.

INDEX 4CH default 00H

Bit	Description
7~0	When IOR Index 4CH is active, the independent GPIO[15-8] will be latch to bit GPI[15-8] . This is Read Only.

INDEX 4DH default 00H

Bit	Description
7~0	Independent GPIO[15-8] signal output and storage register. When write value to this register, bit7~0 will be sent out to GPO[15-8] pins.

INDEX 4EH default 00H

Bit	Description
7~0	Program GPIOE[7-0] , when GPIOE is set up for high , it meanings that independent GPIO will be as GPO[7-0] output pins .

INDEX 4FH default 00H

Bit	Description
7~0	Program GPIOE[15-8] , when GPIOE is set up for high , it meanings that independent GPIO will be as GPO[15-8] output pins .

INDEX 55H default 00H

Bit	Description
7~2	reserved
1~0	SMI timing selection 0 0 : SMI timing support 0 1 : NMI timing support 1 0 : IRQ15 timing support 1 1 : reserved

INDEX 56H default 00H

Bit	Description
7	SMI event signal 0 : disable 1 : enable
6	Software SMI 0 : disable 1 : enable
5~3	reserved
2	PMU state 1 : On 0 : Off
1~0	Power management system mode state 0 0 : ON 0 1 : DOZE 1 0 : STANDBY 1 1 : SUSPEND

INDEX 57H default 00H

Bit	Description
7	DRQ select 1 : selected. If DRQ idle longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
6	FDD select (3F0H-3F7H) 1 : selected. If FDD cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
5	COM select (3F8H-3FFH, 2F8H-2FFH, 3E8H-3EFH, 2E8H-2EEH) 1 : selected. If COM port cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
4	LPT select (378H-37FH, 278H-27FH, 3BCH-3BEH) 1 : selected. If LPT port cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
3	IRQ select 1 : selected. If IRQ idle longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
2	HDD select (1F0H-1F7H) 1 : selected. If HDD cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
1	VGA select (Memory AB region write, 3B0H-3BFH write) 1 : selected. If VGA cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
0	KBD select (60H, 64H) 1 : selected. If KBD cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.

INDEX 58H	default 00H
Bit	Description
7	EXTSW2 active (external SMI switch input, level trigger) 1 : EXTSW2 issues SMI 0 : no SMI from EXTSW2
6	EXTSW1 active (external suspend switch input, level trigger) 1 : EXTSW1 issues SMI 0 : no SMI from EXTSW1
5~2	reserved, must be 0000b.
1	GP1 select 1 : selected. If GP1 cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.
0	GP0 select 1 : selected. If GP0 cannot be accessed longer than mode timer setting. Mode timer time-out will signal. 0 : not selected.

INDEX 59H	default 00H
Bit	Description
7	reserved, must be 0.
6	RTC alarm (IRQ8J) SMI 0 : disable 1 : enable
5	MODE timer time-out signaling SMI 1 : enable 0 : disable
4~0	reserved, must be 00000b.

INDEX 5AH	default 00H
Bit	Description
7	IN signaling SMI 1 : enable 0 : disable
6	DRQ active (select DRQ source by register 5E) signaling SMI 1 : enable 0 : disable
5	IRQ active (select IRQ source by register index 5C,5D) signaling SMI 1 : enable 0 : disable
4	GP1 access (R/W GP1 defined area) signaling SMI 1 : enable 0 : disable
3	GP0 access (R/W GP0 defined area) signaling SMI 1 : enable 0 : disable
2	LPT access (R/W 378H-37FH or 278H-27FH) signaling SMI 1 : enable 0 : disable
1	HDD access (R/W port 1F0H-1F7H) signaling SMI 1 : enable 0 : disable
0	VGA access (W A0000H-BFFFFH, port 3B0H-3BFH) signaling SMI 1 : enable 0 : disable

INDEX 5BH default 00H

Bit	Description
7~5	reserved
4~0	SMI Cause register 0 0 0 0 0 : None 0 0 1 1 0 : Mode Timer Time out 0 1 0 0 0 : IRQ active 0 1 0 0 1 : DRQ active 0 1 0 1 0 : IN access 0 1 1 0 0 : EXTSW1 active (external suspend switch input, level trigger) 0 1 1 0 1 : RTC alarm 0 1 1 1 1 : Software SMI 1 0 0 0 0 : EXTSW2 active (external next SMI switch input, level trigger) 1 0 0 0 1 : VGA access (W A0000H-BFFFFH, port 3B0H-3BFH) 1 0 0 1 0 : HDD access (R/W port 1F0H-1F7H) 1 0 0 1 1 : LPT access (R/W 378H-37FH or 278H-27FH) 1 0 1 0 0 : GP0 access (R/W GP0 defined area) 1 0 1 0 1 : GP1 access (R/W GP1 defined area) Others : reserved

INDEX 5CH default 00H

Bit	Description
	Select source to signal SMI when occur. This selection based on INDEX 5A bit 5 be set.
7	1: IRQ7 event selected 0 : IRQ7 event not selected
6	1: IRQ6 event selected 0 : IRQ6 event not selected
5	1: IRQ5 event selected 0 : IRQ5 event not selected
4	1: IRQ4 event selected 0 : IRQ4 event not selected
3	1: IRQ3 event selected 0 : IRQ3 event not selected
2	1: NMI event selected 0 : NMI event not selected
1	1: IRQ1 event selected 0 : IRQ1 event not selected
0	1: IRQ0 event selected 0 : IRQ0 event not selected

INDEX 5DH default 00H

Bit	Description
	Select source to signal SMI when happening. This selection based on INDEX 5A bit 5 is set.
7	1: IRQ15 event selected 0 : IRQ15 event not selected
6	1: IRQ14 event selected 0 : IRQ14 event not selected
5	1: IRQ13 event selected 0 : IRQ13 event not selected
4	1: IRQ12 event selected 0 : IRQ12 event not selected
3	1: IRQ11 event selected 0 : IRQ11 event not selected
2	1: IRQ10 event selected 0 : IRQ10 event not selected
1	1: IRQ9 event selected 0 : IRQ9 event not selected
0	1: IRQ8 event selected 0 : IRQ8 event not selected

INDEX 5EH default 00H

Bit	Description
	Select source to signal SMI when happened. This selection based on INDEX 5A bit 6 is set.
7	1: DRQ7 event selected 0 : DRQ7 event not selected
6	1: DRQ6 event selected 0 : DRQ6 event not selected
5	1: DRQ5 event selected 0 : DRQ5 event not selected
4	1: DRQ4 event selected 0 : DRQ4 event not selected
3	1: DRQ3 event selected 0 : DRQ3 event not selected
2	1: DRQ2 event selected 0 : DRQ2 event not selected
1	1: DRQ1 event selected 0 : DRQ1 event not selected
0	1: DRQ0 event selected 0 : DRQ0 event not selected

INDEX 64H	default 00H
Bit	Description
7~4	Set the time delay 0 : Timer disable 1-15 : Time count
3	reserved
2	Timer count/reset 1 : Timer count 0 : Timer reset
1~0	Time Base select for Mode timer 0 0 : 1 sec. 0 1 : 10 sec. 1 0 : 1 min. 1 1 : 10 min.

INDEX 66H	default 00H
Bit	Description VGA and IN monitor and signaling SMI. This selection based on INDEX 5A bit 7 is set.
7	IN monitor IRQ3 1: selected 0: not select
6	IN monitor IRQ4 1: selected 0: not select
5	IN monitor IRQ12 1: selected 0: not select
4~2	reserved.
1	VGA monitor I/O write 3B0H-3BFH 1: selected 0: not select
0	VGA monitor memory write A0000H-B0000H 1: selected 0: not select

INDEX 67H	default 00H
Bit	Description
7	SMI event (Read only)
6	EXTSW1 status (Read only)
5	reserved
4	DRQ access (Read only)
3	IRQ access (Read only)
2	EXTSW2 status (Read only)
1-0	EXTSW1/EXTSW2 input polarity setting 00 : disable 01 : rising edge trigger 10 : falling edge trigger 11 : edge trigger

INDEX 68H	default 00H
Bit	Description
7~0	Power ON latched Power Control Initial status from XXD[7-0] D[7-0] : PWR[7-0] control pin status

INDEX 69H	default 00H
Bit	Description
7	reserved, must be 0.
6	Read the timer counter 0 : counter setting 1 : current value
5	reserved, must be 0
4	Double counter time base 0 : disable 1 : enable
3~0	reserved

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INDEX 6AH	default 00H
Bit	Description
7	SUSPEND time-out Mode timer time-out from mode STANDBY to SUSPEND
6	STANDBY time-out Mode timer time-out from mode DOZE to STANDBY
5	DOZE time-out Mode timer time-out from mode ON to DOZE
4~0	reserved, fixed on 0 (Read only)

INDEX 6BH	default 00H
Bit	Description
7	reserved
6	GP1 I/O address 300H-3FFH 0 : disable 1 : enable
5	GP1 I/O address 200H-2FFH 0 : disable 1 : enable
4	GP1 I/O address 100H-1FFH 0 : disable 1 : enable
3~2	Define GP1 I/O address mask A[3-2] respectively. 0 : do not compare this address bit. 1 : compare this address bit.
1	GP0 memory address 0 : disable 1 : enable
0	GP1 I/O address 0 : disable 1 : enable

INDEX 6CH	default 00H
Bit	Description
7~0	Define GP0 memory address A[23-16]

INDEX 6DH	default 00H
Bit	Description
7~0	Define GP0 memory address A[23-16] mask bits respectively. 1 : compare this address bit. 0 : do not compare this address bit.

INDEX 6EH	default 00H
Bit	Description
7~2	reserved, must be 000000b
1~0	Define GP0 memory address A[25-24].

INDEX 6FH	default 00H
Bit	Description
7~2	reserved, must be 000000b
1~0	Define GP0 memory address A[25-24] mask bits respectively. 1 : compare this bit 0 : do not compare this bit

INDEX 70H	default 00H
Bit	Description
7~0	Define GP1 I/O port address SA[9-2]

INDEX 71H	default 00H
Bit	Description
7~5	reserved
4~2	Define Mode LED on/off period 0 0 0 : 0.1 sec 0 0 1 : 0.2 sec 0 1 0 : 0.4 sec 0 1 1 : 0.8 sec 1 0 0 : 1.0 sec 1 0 1 : 2.0 sec 1 1 0 : 4.0 sec 1 1 1 : 8.0 sec
1~0	Define Mode LED duty cycle 0 0 : disable 0 1 : 25% 1 0 : 50% 1 1 : 75%

INDEX 72H	default 00H
Bit	Description
7~0	Shadow I/O port for port 70H data

INDEX 73H	default 00H
Bit	Description
7~0	Power Control status output command Write to this port will generate enpower pulse to update power control status.

Section 5 : Programming Guide

5.1 Basic Procedure and Macro Definition

a) Delay

```
IO_Delay MACRO
        jcxz  $+2
        jcxz  $+2
        ENDM
```

b) Unlock chipset• configure registers

```
Open_Chip MACRO
        mov  al, 013h
        out   022h, al
        IO_Delay
        mov  al, 0c5h
        out   023h, al
        IO_Delay
        ENDM
```

c) Lock chipset• configure registers

```
Close_Chip MACRO
        mov  al, 013h
        out   022h, al
        IO_Delay
        mov  al, 000h
        out   023h, al
        IO_Delay
        ENDM
```

d) Write data to configure register

```
; INPUT :    AH      -       INDEX#
; INPUT :    AL      -       Data
; ACTION :   Write the value of AL into the value of AH INDEX
; Interrupt controller and Stack are available
Write_To_Chip PROCEDURE
        cli
        push ax
        Open_Chip
        pop  ax
        out   022h, al
        IO_Delay
        xchg ah, al
        out   023h, al
        IO_Delay
        xchg ah, al
        push ax
        Close_Chip
        pop  ax
        sti
        ret
        ENDP
```

e) Read data from configure register

```
; INPUT :     AL      -       INDEX#
; OUTPUT :  AL      -       Data
; ACTION :   Read data from the value of AL INDEX
; Interrupt controller and Stack are available
Read_From_Chip PROC
        cli
        push ax
        Open_Chip
        pop  ax
        out  022h, al
        IO_Delay
        in   al, 023h
        IO_Delay
        push ax
        Close_Chip
        pop  ax
        sti
        ret
        ENDP
```

5.2 Detection and Setting of Fast Page Mode and EDO DRAMs

```
; BD0 must be pulled high 10K
; Stack must be available
; all routines in this section must be executed at ROM access

DRAM_Type_Detection:
        mov  ax, 01010h                 ; Set mode 5 for DRAM detection
        call Read_From_Chip
        and  al, 00000111b
        or   al, 01010000b
        xchg ah, al
        call Write_To_Chip

        mov  ax, 03c3ch                 ; Set the bit 1 of INDEX 3Ch to '1'
        call Read_From_Chip             ; to enable EDO DRAM timing detect
        or   al, 00000010b              ; mode.
        xchg ah, al
        call Write_To_Chip

        push ds
        mov  ax, 0h
        mov  ds, ax
        mov  ds: word ptr[0h], 0aaaah
        mov  ds: word ptr[1000h], 05555h    ; dummy write
        cmp  ds: word ptr[0h], 0aaaah
        je   Is_EDO_type_DRAM
```

```
Is_Fast_Page_Mode_Type_DRAM :
        mov   ax, 03c3ch
        call  Read_From_Chip
        and   al, 11111101b             ; Disable EDO DRAM timing detect
        xchg  ah, al                    ; mode
        call  Write_To_Chip
        jmp   Finish_DRAM_Type_Detection

Is_EDO_Type_DRAM:
        mov   ax, 03c3ch
        call  Read_From_Chip
        and   al, 11111101b             ; Disable EDO DRAM timing detect
        xchg  ah, al                    ; mode
        call  Write_To_Chip

        mov   ax, 03737h
        call  Read_From_Chip
        or    al, 00000001b             ; Set EDO DRAM mode
        xchg  ah, al
        call  Write_To_Chip

Finish_DRAM_Type_Detection:
        pop   ds
        ret
```

5.3 Memory Auto Sizing

```
big_gdt_descriptor label fword
        dw      big_gdt_end - big_gdt - 1   ; limit of gdt
        dw      offset big_gdt
        db      0fh
        db      93h
        dw      0000h

big_gdt label qword
        dq      0
        dq      008f93000000ffffh
        dq      000093000000ffffh
big_gdt_end equ $

mem_config_table label word
        ;       memory mode                     total
        ;       type            pattern         memory          Type
        dw      0011h,          0000h,          0001h,          ; 0
        dw      1111h,          0010h,          0002h,          ; 1
        dw      0311h,          0020h,          0003h,          ; 2
        dw      3311h,          0030h,          0005h,          ; 3
        dw      0511h,          0040h,          0009h,          ; 4
        dw      0002h,          0050h,          0001h,          ; 5
        dw      0022h,          0060h,          0002h,          ; 6
        dw      0322h,          0070h,          0004h,          ; 7
        dw      3322h,          0080h,          0006h,          ; 8
        dw      0522h,          0090h,          000ah,          ; 9
        dw      5522h,          00a0h,          0012h,          ; 10
        dw      0032h,          00b0h,          0003h,          ; 11
        dw      0332h,          00c0h,          0005h,          ; 12
        dw      0052h,          00d0h,          0009h,          ; 13
        dw      0003h,          00e0h,          0002h,          ; 14
        dw      0033h,          00f0h,          0004h,          ; 15
        dw      0333h,          0008h,          0006h,          ; 16
        dw      3333h,          0018h,          0008h,          ; 17
        dw      0533h,          0028h,          000ch,          ; 18
        dw      5533h,          0038h,          0014h,          ; 19
        dw      0053h,          0048h,          000ah,          ; 20
        dw      0553h,          0058h,          0012h,          ; 21
        dw      5553h,          0068h,          001ah,          ; 22
        dw      0004h,          0078h,          0004h,          ; 23
        dw      0044h,          0088h,          0008h,          ; 24
        dw      5544h,          0098h,          0018h,          ; 25
        dw      0054h,          00a8h,          000ch,          ; 26
        dw      0005h,          00b8h,          0008h,          ; 27
        dw      0055h,          00c8h,          0010h,          ; 28
        dw      0555h,          00d8h,          0018h,          ; 29
        dw      5555h,          00e8h,          0020h,          ; 30
        dw      0066h,          00f8h,          0040h,          ; 31

  ; Stack must be available
  ; all routines in this section must be executed at ROM access
```

```
Auto_DRAM_sizing :

        call    DRAM_Type_Detection         ; Detect and set the EDO DRAM

        ; enable 8042 address line 20 here

        .386p
        mov   eax, cr0                      ; Set PE
        or    al, 01h                       ; Enter protected mode
        mov   cr0, eax

        cli

        lgdt    cs: big_gdt_descriptor
        jmp     short enter_protected_mode

enter_protected_mode:
        mov   ax, 0008h
        mov   ds, ax

        mov   ax, 01010h                    ; Set mode 30 for DRAM sizing
        call  Read_From_Chip
        and   al, 00000111b
        or    al, 11101000b
        xchg  ah, al
        call  Write_To_Chip

        xor   dx, dx                        ; store DRAM mode
        mov   esi, 3000h                    ; A13, A12 enable - bank 3

sizing_bank_23:
        mov   edi, 800h                     ; A11
        and   dl, 0f0h
        or    dl, 5                         ; 5 --- 4M
        mov   ds: word ptr[esi+edi], 0aa99h
        mov   ds: word ptr[esi], 099aah     ; dummy write
        cmp   ds: word ptr[esi+edi], 0aa99h
        jz    sizing_bank_23_end            ; 4M, go to test next bank

        mov   edi, 400h                     ; A10
        and   dl, 0f0h
        or    dl, 3                         ; 3 --- 1M
        mov   ds: word ptr[esi+edi], 0bb88h
        mov   ds: word ptr[esi], 088bbh     ; dummy write
        cmp   ds: word ptr[esi+edi], 0bb88h
        jz    sizing_bank_23_end            ; 1M, go to test next bank

        mov   edi, 2h                       ; A1
        and   dl, 0f0h
        or    dl, 1                         ; 1 --- 256K
        mov   ds: word ptr[esi+edi], 0cc77h
        mov   ds: word ptr[esi], 077cch     ; dummy write
        cmp   ds: word ptr[esi+edi], 0cc77h
        jz    sizing_bank_23_end            ; 256K, go to test next bank

        and   dl, 0f0h                      ; none in this bank

sizing_bank_23_end:
        cmp   esi, 2000h
```

```
                jz      short sizing_bank_01_begin      ; finish sizing bank 3 and 2
                sub     esi, 1000h
                shl     dx, 4
                jmp     sizing_bank_23                  ; go to sizing bank 2

sizing_bank_01_begin:
                mov     ax, 01010h                      ; Set mode 31 for DRAM sizing
                call    Read_From_Chip
                and     al, 00000111b
                or      al, 11111000b
                xchg    ah, al
                call    Write_To_Chip

sizing_bank_01:
                shl     dx, 4                           ; next bank

                mov     edi, 1000h                      ; A12
                and     dl, 0f0h
                or      dl, 6                           ; 6 --- 16M
                mov     ds: word ptr[esi+edi], 0dd66h
                mov     ds: word ptr[esi], 066ddh       ; dummy write
                cmp     ds: word ptr[esi+edi], 0dd66h
                jz      sizing_bank_01_end              ; 16M, go to test next bank

                mov     edi, 800h                       ; A11
                and     dl, 0f0h
                or      dl, 5                           ; 5 --- 4M
                mov     ds: word ptr[esi+edi], 0ee55h
                mov     ds: word ptr[esi], 055eeh       ; dummy write
                cmp     ds: word ptr[esi+edi], 0ee55h
                jz      sizing_bank_01_end              ; 4M, go to test next bank

                mov     edi, 400h                       ; A10
                and     dl, 0f0h
                or      dl, 3                           ; 3 --- 1M
                mov     ds: word ptr[esi+edi], 0ff44h
                mov     ds: word ptr[esi], 044ffh       ; dummy write
                cmp     ds: word ptr[esi+edi], 0ff44h
                jz      short is_1or2M                  ; 1 or 2M, go to is_1or2M to check

                mov     edi, 2                          ; A1
                and     dl, 0f0h
                or      dl, 1                           ; 1 --- 256K
                mov     ds: word ptr[esi+edi], 012abh
                mov     ds: word ptr[esi], 0ab12h       ; dummy write
                cmp     ds: word ptr[esi+edi], 012abh
                jz      short is_2or5K                  ; 256 or 512K, go to is_2or5K to check

                and     dl, 0f0h                        ; none in this bank
                jmp     short sizing_bank_01_end
```

```
is_1or2M:
        mov   edi, 1000000                  ; A24
        mov   ds: word ptr[esi+edi], 034cdh
        mov   ds: word ptr[esi], 0ed34h     ; dummy write
        cmp   ds: word ptr[esi+edi], 034cdh
        jnz   short sizing_bank_01_end      ; 1M
        and   dl, 0f0h
        or    dl, 4                         ; 2M
        jmp   short sizing_bank_01_end

is_2or5K:
        mov   edi, 100000                   ; A20
        mov   ds: word ptr[esi+edi], 056efh
        mov   ds: word ptr[esi], 0ef56h     ; dummy write
        cmp   ds: word ptr[esi+edi], 056efh
        jnz   short sizing_bank_01_end      ; 256K
        and   dl, 0f0h
        or    dl, 2                         ; 512K

sizing_bank_01_end:
        cmp   esi, 0
        jz    short sizing_memory_end
        mov   esi, 0                        ; bank 0
        jmp   sizing_bank_01

sizing_memory_end:
        mov   ax, 010h                      ; reset descriptor
        mov   ds, ax

        mov   eax, cr0                      ; reset PE
        and   al, 0feh
        mov   cr0, eax
        jmp   short enter_real_mode

enter_real_mode:
        .286p

        ; disable 8042 address line 20 here

        mov   si, offset cgroup: mem_config_table
        mov   cx, 32

check_mode :
        mov   ax, cs: word ptr[si]
        cmp   dx, ax
        jz    short check_mode_end
        add   si, 6
        loop  check_mode

        ; Display memory error here
        ;
        ; if  dx = 0001, set mode 5 for 512K DRAM
        ;
```

```
check_mode_end:
        mov   bx, cs: word ptr[si+2]

        mov   ax, 01010h                    ; Set DRAM Mode
        call  Read_From_Chip
        and   al, 00000111b
        or    al, bl
        xchg  ah, al
        call  Write_To_Chip

        ;
        ; Do your memory remapping setting here.
        ;
        ; Use the total DRAM size to check whether the remapping is
        ; allowable or not.
        ; Use the total DRAM size to set the bit 7-4 of INDEX 12h Split address.
        ; Select the remap mode by setting the bit 1 of INDEX 11h.
```

5.4 Remapping Memory

If enable memory remap(INDEX 11h, bit 2), we have two choices: split or move-out. We can use the split mode when the size of the DRAM is less than 16M owing to the limitation of hardware. In this way, the available memory is increased. When the memory size is less than 16M, we can also choose the move-out mode. Therefore, we should get the DRAM size by the Auto_DRAM_Sizing routine. The details of setting the configure registers are described as follows :

```
; Get the total memory size to bl
;
; 1). Get the total memory size from Auto_DRAM_Sizing

        mov   bl, cs: byte ptr[si+4]

; or 2). Using the following routine to get the total memory size from reading DRAM mode

        mov   al, 010h
        call  Read_From_Chip
        and   al, 11111000b
        xor   dx, dx
        or    dl, al
        mov   si, offset cs: mem_config_table
        mov   cx, 32
check_mem_mode:
        mov   ax, cs: word ptr[si+2]
        cmp   dx, ax
        jz    short check_mem_mode_end
        add   si, 6
        loop  check_mem_mode
check_mem_mode_end:
        mov   bl, cs: byte ptr[si+4]

        cmp   bl, 16
        ja    do_remap_memory

; if bl >= 16 (the memory size is equal to or greater than 16M ), disable memory remapping.
        mov   ax, 01111h                    ; Disable memory remapping
        call  Read_From_Chip
        and   al, 11111011b
        xchg  ah, al
        call  Write_To_Chip
```

```
; Otherwise, doing memory remap in the following routine
; 1) We would like to choose move-out mode
        mov   ax, 01111h                ; Enable memory remapping
        call  Read_From_Chip            ; Select move-out mode
        and   al, 11111001b
        or    al, 00000110b
        xchg  ah, al
        call  Write_To_Chip

        mov   ax, 01212h                ; Set Split address SP[23-20]
        call  Read_From_Chip            ; to [1111]
        and   al, 00001111b
        or    al, 11110000b
        xchg  ah, al
        call  Write_To_Chip

; or 2) We would like to choose split mode
        mov   ax, 01111h                ; Enable memory remapping
        call  Read_From_Chip            ; Select split mode
        and   al, 11111001b
        or    al, 00000100b
        xchg  ah, al
        call  Write_To_Chip

        mov   ax, 01212h                ; Set Split address SP[23-20]
        call  Read_From_Chip            ; to [1111]
        and   al, 00001111b
        shl   bl, 4                     ; bl - total memory size
        or    al, bl
        xchg  ah, al
        call  Write_To_Chip
```

5.5 Interrupt controller edge/level trigger programming

The default setting of M6117D interrupt controller is edge trigger disregarding the value of ICW1. M6117D has the ability of setting each IRQ to be edge or level trigger by decoding I/O ports 04d0h and 04d1h.

To enable this feature, set the bit 2 of INDEX 3Ch to '1'.

```
        mov   ax, 03c3ch                ; Enable IRQ level trigger selection
        call  Read_From_Chip
        or    al, 00000100b
        xchg  ah, al
        call  Write_To_Chip
```

Then the I/O port 04d0h and 04d1h can set the corresponding IRQ to be level trigger.

```
I/O port 04d0h    -    Interrupt controller 1
        bit 7  -  IRQ7
        bit 6  -  IRQ6
          :
        bit 1  -  IRQ1
        bit 0  -  IRQ0
I/O port 04d1h    -    Interrupt controller 2
        bit 7  -  IRQ15
        bit 6  -  IRQ14
          :
        bit 1  -  IRQ9
        bit 0  -  IRQ8
```

To enable IRQ10 to be level trigger, use

```
mov  dx, 04d1h
in   al, dx
IO_Delay
or   al, 00000100          ; bit 2 - IRQ10
out  dx, al
IO_Delay
```

5.6 PMU Programming Guide

5.6.1 Power Management Mode Selection

If any event happens, M6117D will check the setting of INDEX 55h and INDEX 38h to generate a signal.

1) SMI support :

```
mov  ax, 05555h
call Read_From_Chip
and  al, 11111100b         ; SMI support
xchg ah, al
call Write_To_Chip
```

2) NMI support :

```
mov  ax, 05555h
call Read_From_Chip
and  al, 11111100b
or   al, 00000001b         ; NMI support
xchg ah, al
call Write_To_Chip
```

3) IRQ15 support:

```
mov  ax, 05555h
call Read_From_Chip
and  al, 11111100b
or   al, 00000010b         ; IRQ15 support
xchg ah, al
call Write_To_Chip
```

4) Other IRQs support: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14.

```
mov   ax, 05555h
call  Read_From_Chip
or    al, 00000011b                ; IRQ3, IRQ4,•RQ14 support
xchg  ah, al
call  Write_To_Chip
```

Then set the bit 3-0 of INDEX 38h to IRQ number.

```
mov   ax, 03838h
call  Read_From_Chip
and   al, 11110000b
or    al, 00000011b                ; IRQ3 support
(or   al, 00000100b                ; IRQ4 support
(or   al, 00001110b                ; IRQ14 support
xchg  ah, al
call  Write_To_Chip
```

5.6.2 Structure of Power Management routine

```
mov   ax, 05656h
call  Read_From_Chip
and   al, 01111111b                ; disable SMI signal
xchg  ah, al
call  Write_To_Chip

; read event from INDEX 5bh
mov   al, 05bh
call  Read_From_Chip
; check the bit4-0 of INDEX 5bh
; disable PMU state
mov   ax, 05656h
call  Read_From_Chip
and   al, 11111011b                ; disable PUM state
xchg  ah, al
call  Write_To_Chip

; disable original event
; by clearing INDEX 58h, 59h, 5ah
;
; do your power management routine here
;

; set the condition of your next power management event
; by setting INDEX 57h, 58h, 59h, 5ah, 5ch, 5dh, 5eh, 64h, 66h, 67h, 69h, 6bh, 6ch, 6dh,
; 6eh, 6f, 70h
```

5.6.3 Power management example

In the following example, use
LPOETW(INDEX#, DATA) to write chipset• configure register and
LPORTR(INDEX#) to read chipset• configure register

Example 1 : Mode Translation

```
                        /* The DOZE, STANDBY, SUSPEND modes are defined by the BIOS */
LPORTW(056h,084h);      /* Enable SMI, PMU and set the system state at ON mode */
LPORTW(057h,008h);      /* Monitor IRQs in this example */
LPORTW(059h,020h);      /* Enable MODE timer */
LPORTW(064h,067h);      /* Set the time base of the MODE timer as 60 min */
                        /* SMIJ will be generated if no IRQ is active during 60 min */
                        /* Wait for the assertion of SMIACKJ */
LPORTW(056h,004h);      /* Deassert SMIJ */
LPORTR(05Bh);           /* To read the SMI cause */
                        /* It should be the MODE timer time-out in this example */
LPORTR(06Ah);           /* Read the time-out status */
                        /* Start SMI routine */
LPORTW(059h,000h);      /* Clear MODE time-out event */
LPORTW(05Ah,080h);      /* Set IN(standard input) as a wake-up event */
LPORTW(056h,084h);      /* Enable SMI again */
DB 0D6h ;               /* End SMI routine */
DB 0E6h ;               /* RETPM */
```

Example 2 : External Switch

```
LPORTW(056h,084h);      /* Enable SMI and PMU function */
LPORTW(067h,003h);      /* Set external switch both low-to-high and high-to-low active */
LPORTW(058h,000h);      /* Clear external switch */
LPORTW(058h,040h);      /* Enable external switch */
                        /* SMI is generated when external switch is pushed */
                        /* Wait for the assertion of SMIACKJ */
LPORTR(05Bh);           /* To find out the SMI event is caused by which time-out event */
                        /* It should be the external switch active in this example */
LPORTR(067h);           /* Check the external switch status */
                        /* Start SMI routine */
LPORTW(058h,000h);      /* Clear external switch */
LPORTW(058h,040h);      /* Enable external switch */
LPORTW(05Ah,080h);      /* Set IN(standard input) as a wake-up event */
LPORTW(056h,084h);      /* Enable SMI again */
DB 0D6h                 /* End SMI routine */
DB 0E6h                 /* RETPM */
```

Example 3: Usage of the IN Group

IN group is used to monitor the activity of the standard input devices.

IN group is defined as:

IRQ1: default for keyboard
IRQ12: optional for PS/2 mouse (index 66_D5)
IRQ4: optional for COM1 mouse (index 66_D6)
IRQ3: optional for COM2 mouse (index 66_D7)

IN group timer time-out:

(1) Generate power control signal to turn off the screen
(2) Enter SMM by asserting SMIJ

IN group access:

(1) Generate power control signal to turn on the screen
(2) Enter SMM by asserting SMIJ

Hence, monitoring the IN group activity can be used to implement the function of the •creen saver". Besides, it will not impact the performance of the running program, instead the whole power can be reduced dramatically.

Example 4 : Software SMI Event

```
LPORTW(0x56,0xC4);      /* Enable SMI and PMU function, and enable software SMI */
                        /* SMIJ is asserted */
                        /* Wait for the assertion of SMIADSJ */
LPORTR(0x5B);           /* Read SMI cause, it should be software SMI */
LPORTW(0x56,0x04);      /* Deassert SMIJ */
                        /* Start SMI routine */
LPORTW(0x56,0x84);      /* Enable SMI again */
DB 0D6h;                /* End SMI routine */
DB 0E6h;                /* RETPM */
```

Example 5 : SMM Remap Start Address

```
LPORTW(0x20,0xB0);              /* Remap start address to F region, no shadow */
MOV eax, 000F0000h              /* start address = 000F0000 */
DB 0D6h,0CAh,03h,0A0h  /* Load EA0 to ultra SR register*/
DB 0D6h,0C8h,03h,0A0h           /* Load ultra SR register to EA0 */
DB 0F1h                         /* BRKPM, instruction to enter SMM mode */

LPORTW(0x20,0x90);              /* Remap start address to AB region, shadow */
mov eax, 000A0000h              /* start address = 000A0000 */
DB 0D6h,0CAh,03h,0A0h           /* Load EA0 to ultra SR register*/
DB 0D6h,0C8h,03h,0A0h           /* Load ultra SR register to EA0 */
DB 0F1h                         /* BRKPM, instruction to enter SMM mode */

LPORTW(0x20,0xA0);              /* Remap start address to E region, shadow */
mov eax, 000E0000h              /* start address = 000E0000 */
DB 0D6h,0CAh,03h,0A0h           /* Load EA0 to ultra SR register*/
DB 0D6h,0C8h,03h,0A0h           /* Load ultra SR register to EA0 */
DB 0F1h                         /* BRKPM, instruction to enter SMM mode */

LPORTW(0x20,0xB8);              /* Remap start address to F region, shadow */
mov eax, FFFF0000h              /* start address = FFFF0000 */
DB 0D6h,0CAh,03h,0A0h           /* Load EA0 to ultra SR register*/
DB 0D6h,0C8h,03h,0A0h           /* Load ultra SR register to EA0 */
DB 0F1h                         /* BRKPM, instruction to enter SMM mode */
```

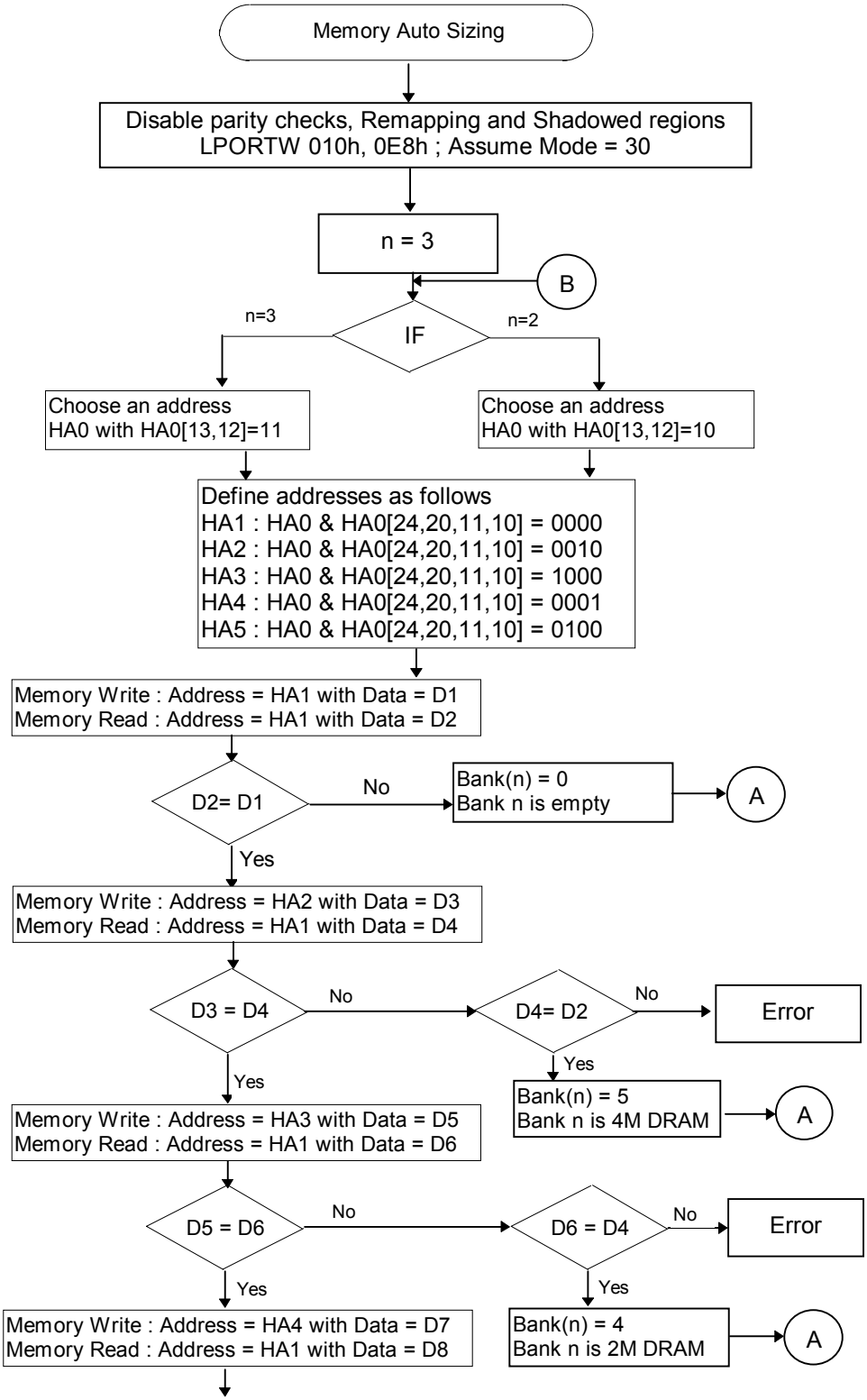
Example 6 : Stop Internal CPU Clock

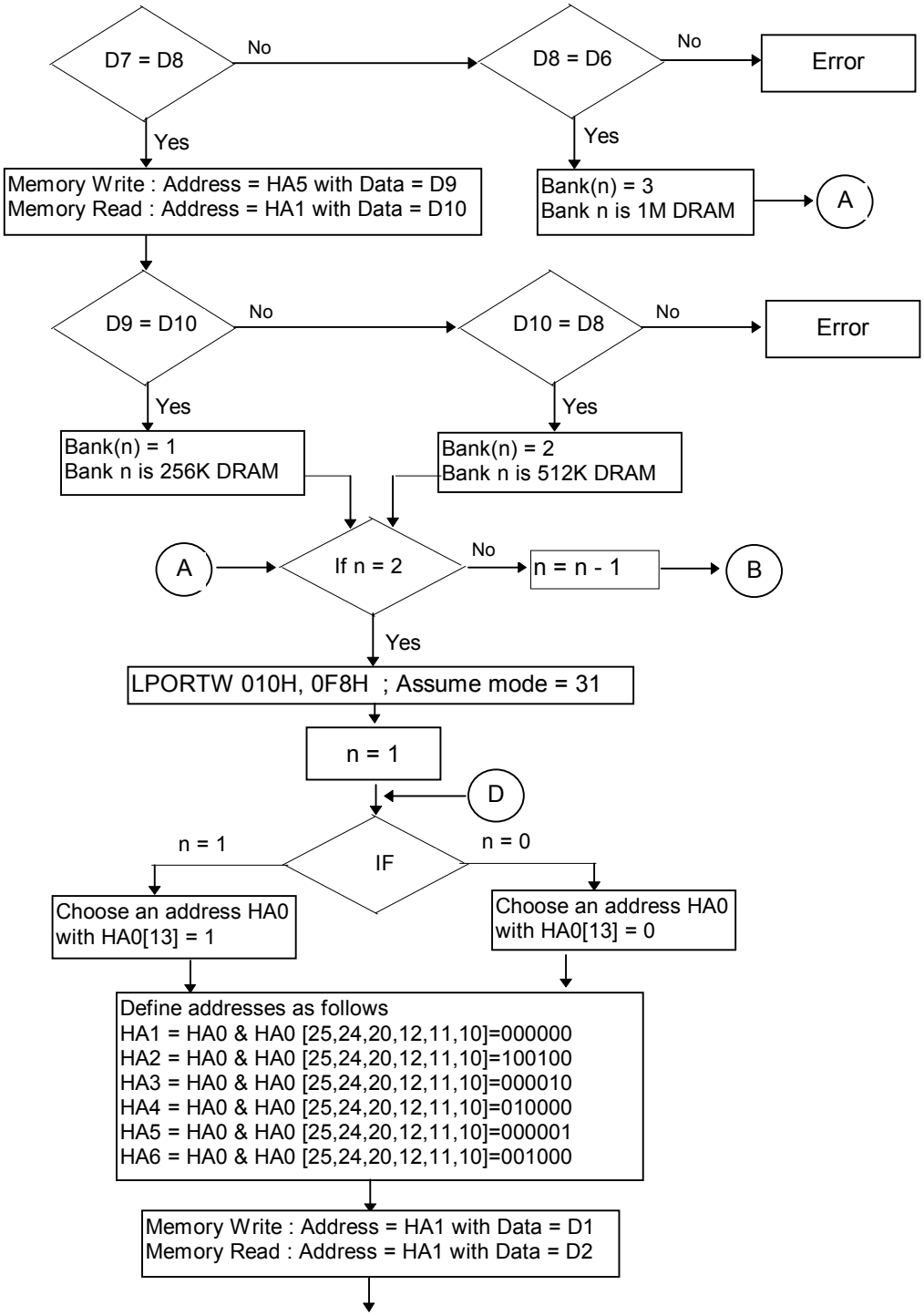
```
mov eax, 00080000h              /* Set  Power Control Register Clock Stop Bit = 1 */
DB 0D6h,0FAh,03h,02h            /* MOV PWRCR, EA0 , where PWRCR is Power control register*/
hlt                             /* Stop internal CPU clock */
                                /* Wake up by INTR, NMI */
```

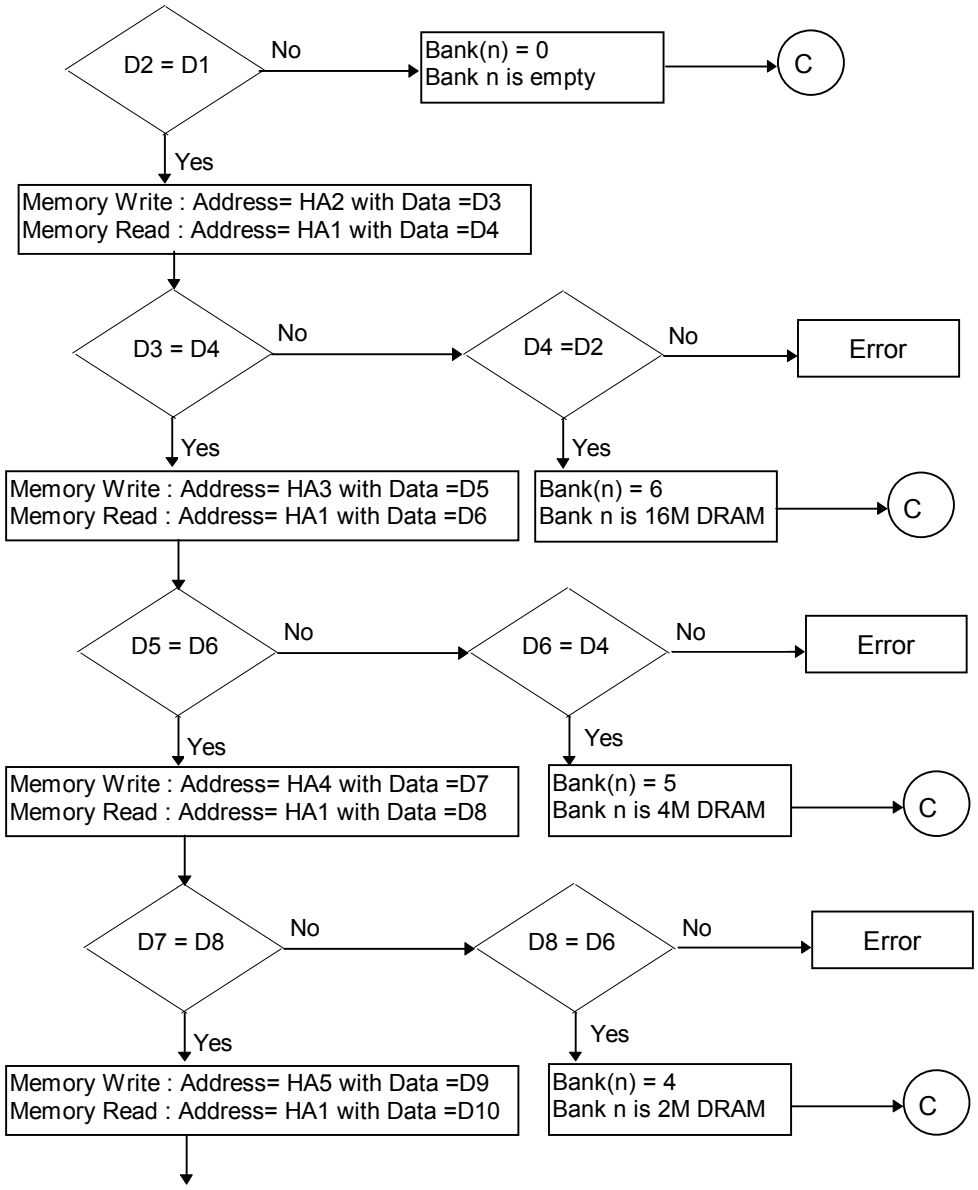
5.7 Flowcharts

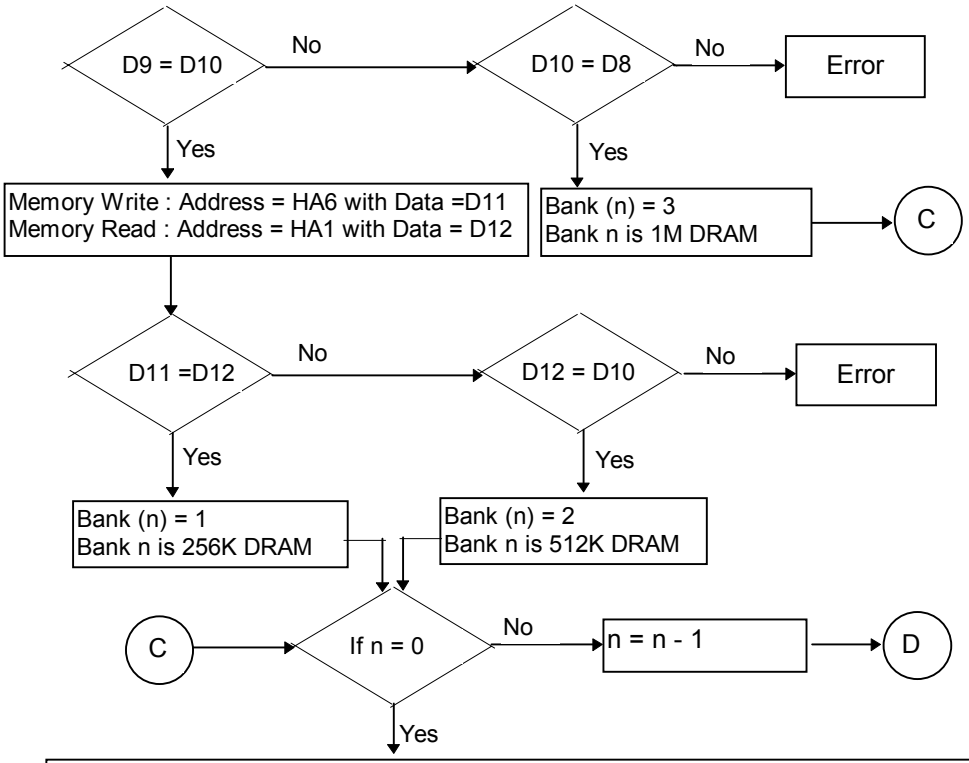
Note : The following notations below have the following meanings.
HAi (where I is an integer) denotes a specific CPU address.
HAi[j] denotes the jth bit of the address lines HAi.
•Ai & HAi[j] = K denote the specific address Hai is with a binary value K assigned to the jth bit.

A. Flowchart of Detecting Memory Mode



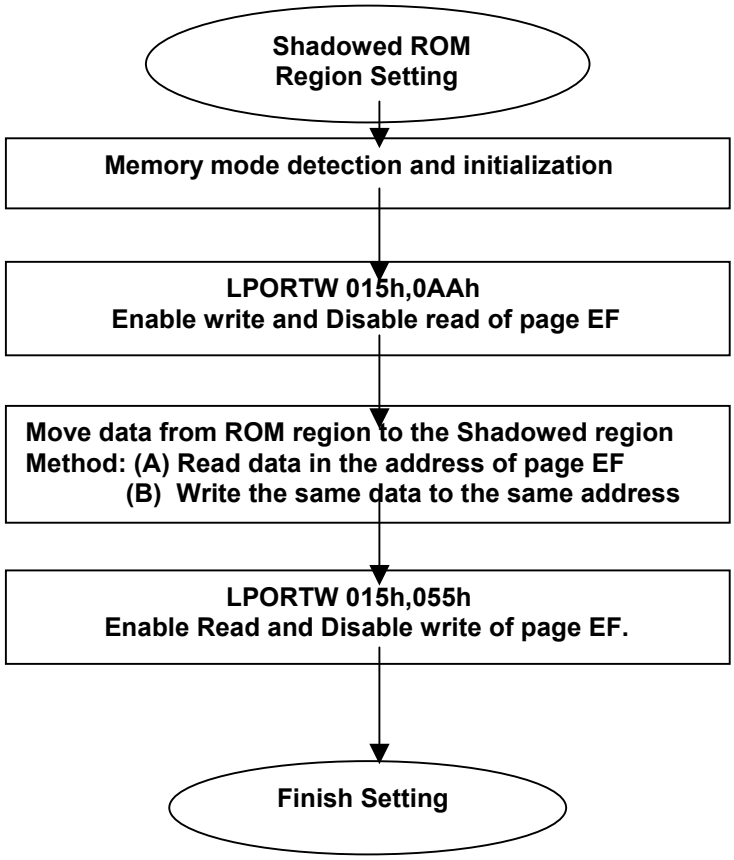

D7 = D8
No
D8 = D6
No
Error
Yes
Yes
Memory Write : Address = HA5 with Data = D9
Memory Read : Address = HA1 with Data = D10
Bank(n) = 3
Bank n is 1M DRAM
A
D9 = D10
No
D10 = D8
No
Error
Yes
Yes
Bank(n) = 1
Bank n is 256K DRAM
Bank(n) = 2
Bank n is 512K DRAM
A
If n = 2
No
n = n - 1
B
Yes
LPORTW 010H, 0F8H ; Assume mode = 31
n = 1
D
n = 1
IF
n = 0
Choose an address HA0
with HA0[13] = 1
Choose an address HA0
with HA0[13] = 0
Define addresses as follows
HA1 = HA0 & HA0 [25,24,20,12,11,10]=000000
HA2 = HA0 & HA0 [25,24,20,12,11,10]=100100
HA3 = HA0 & HA0 [25,24,20,12,11,10]=000010
HA4 = HA0 & HA0 [25,24,20,12,11,10]=010000
HA5 = HA0 & HA0 [25,24,20,12,11,10]=000001
HA6 = HA0 & HA0 [25,24,20,12,11,10]=001000
Memory Write : Address = HA1 with Data = D1
Memory Read : Address = HA1 with Data = D2


D2 = D1
No
Bank(n) = 0
Bank n is empty
C
Yes
Memory Write : Address= HA2 with Data =D3
Memory Read : Address= HA1 with Data =D4
D3 = D4
No
D4 =D2
No
Error
Yes
Yes
Memory Write : Address= HA3 with Data =D5
Memory Read : Address= HA1 with Data =D6
Bank(n) = 6
Bank n is 16M DRAM
C
D5 = D6
No
D6 = D4
No
Error
Yes
Yes
Memory Write : Address= HA4 with Data =D7
Memory Read : Address= HA1 with Data =D8
Bank(n) = 5
Bank n is 4M DRAM
C
D7 = D8
No
D8 = D6
No
Error
Yes
Yes
Memory Write : Address= HA5 with Data =D9
Memory Read : Address= HA1 with Data =D10
Bank(n) = 4
Bank n is 2M DRAM
C

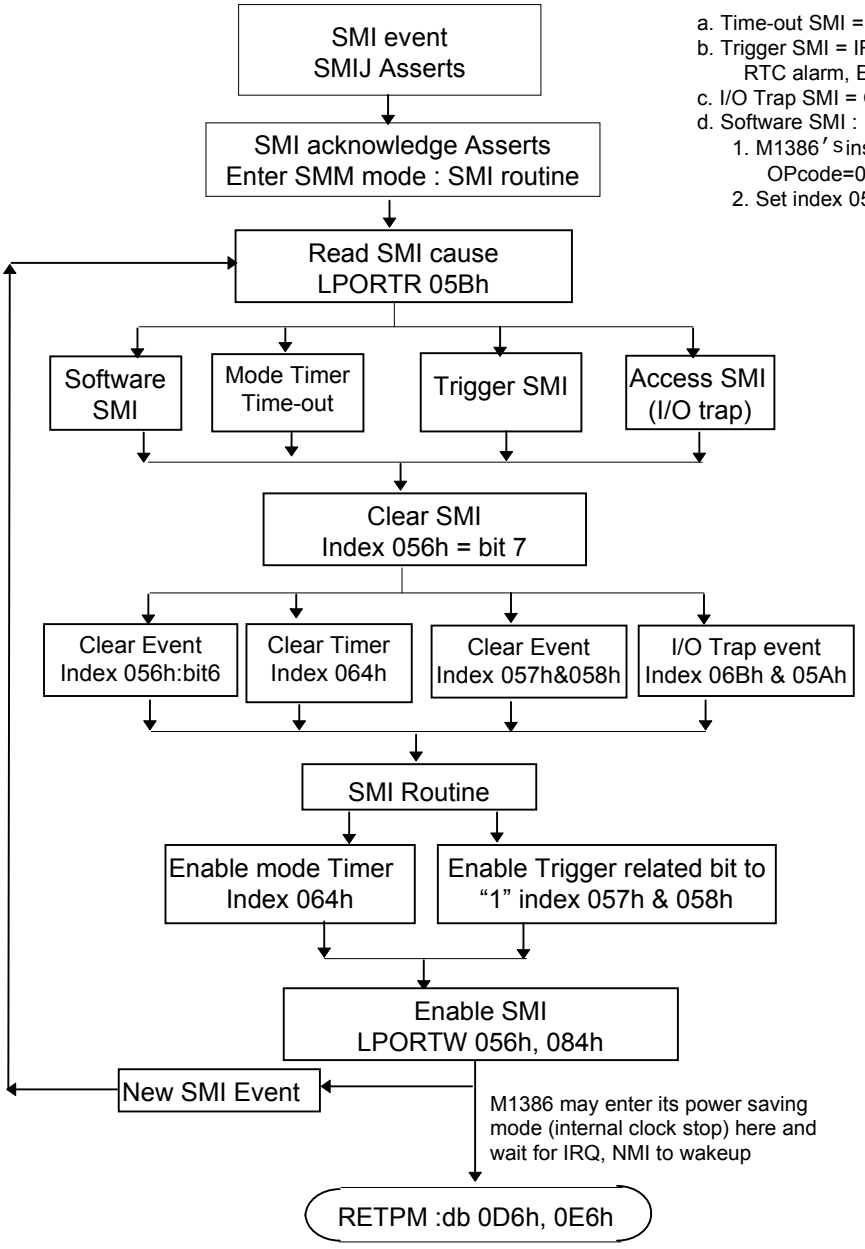


Case Bank (3-0)	
0,0,1,1 : Memory Mode = 0	3,3,3,3 : Memory Mode = 17
1,1,1,1 : Memory Mode = 1	0,5,3,3 : Memory Mode = 18
0,3,1,1 : Memory Mode = 2	5,5,3,3 : Memory Mode = 19
3,3,1,1 : Memory Mode = 3	0,0,5,3 : Memory Mode = 20
0,5,1,1 : Memory Mode = 4	0,5,5,3 : Memory Mode = 21
0,0,0,2 : Memory Mode = 5	5,5,5,3 : Memory Mode = 22
0,0,2,2 : Memory Mode = 6	0,0,0,4 : Memory Mode = 23
0,3,2,2 : Memory Mode = 7	0,0,4,4 : Memory Mode = 24
3,3,2,2 : Memory Mode = 8	5,5,4,4 : Memory Mode = 25
0,5,2,2 : Memory Mode = 9	0,0,5,4 : Memory Mode = 26
5,5,2,2 : Memory Mode = 10	0,0,0,5 : Memory Mode = 27
0,0,3,2 : Memory Mode = 11	0,0,5,5 : Memory Mode = 28
0,3,3,2 : Memory Mode = 12	0,5,5,5 : Memory Mode = 29
0,0,5,2 : Memory Mode = 13	5,5,5,5 : Memory Mode = 30
0,0,0,3 : Memory Mode = 14	0,0,6,6 : Memory Mode = 31
0,0,3,3 : Memory Mode = 15	Others : Type is undefined
0,3,3,3 : Memory Mode = 16	

B. Flowchart of Enabling the Shadowed Regions



C. SMI Control Flowchart



a. Time-out SMI = Mode Time-out
b. Trigger SMI = IRQ,DRQ,IN_device access, RTC alarm, EXTSW
c. I/O Trap SMI = GP0, GP1,LPT,HDD,VGA
d. Software SMI :
   1. M1386's instruction OPcode=0F1h
   2. Set index 056h : bit 6

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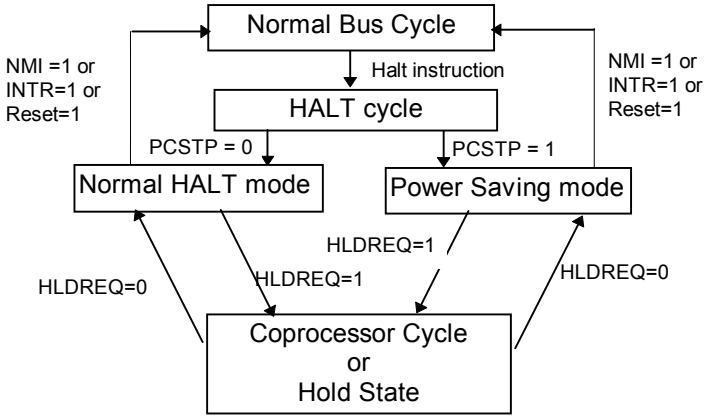
4. M6117D Power Saving Mode



Question : How to set PCSTP ? (Power Clock Stop)

Answer : MOV EAX, 00080000h
DB 0D6h, 0FAh, 03h, 02h
/* MOV PWRCR, EA0 */

MA Table

DRAM mode	DRAM type	Bank	DRAM addr	MA0 MA1 MA2	MA3 MA4 MA5	MA6 MA7 MA8	MA9 MA10 MA11	Enable Bank
0	256K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1		A10
1	256K	0-3	row column	PA20 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1		A11, A10
2	256K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 A18 PA19 A8 A9 A1		A10
	1M	2	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 ___ ___ A10 ___ ____	
3	256K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1		A10
	1M	2,3	row column	A21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 ___ ____ A10 ___ ____	A11
4	256K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1		A10
	4M	2	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 ___ A10 A11 ___	
5	512K	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA19 ___ ___	
6	512K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 ___ ___	A10
7	512K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 ___ ___	A10
	1M	2	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 ___ ___ A10 ___ ___	
8	512K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 _____	A10
	1M	2,3	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 ___ ___ A10 ___ ___	A11
9	512K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 __ ___	A10
	4M	2	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 __ A10 A11 ___	
10	512K	0,1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 __ __	A10
	4M	2,3	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 ___ A10 A11 ___	A12

MA Table (continued)

DRAM mode	DRAM type	Bank	DRAM addr	MA0 MA1 MA2	MA3 MA4 MA5	MA6 MA7 MA8	MA9 MA10 MA11	Enable Bank
11	512K	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 A10 A8 A9 A1	PA19	
	1M	1	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	
12	512K	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 A18 A10 A8 A9 A1	PA19	
	1M	1,2	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	A11
13	512K	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 A10 A8 A9 A1	PA19	
	4M	1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	
14	1M	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	
15	1M	0,1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	A11
16	1M	0,1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	A11
	1M	2	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	
17	1M	0-3	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	A12,A11
18	1M	0,1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	A11
	4M	2	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	
19	1M	0,1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	A11
	4M	2,3	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 A10 A11	A12
20	1M	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	
	4M	1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	

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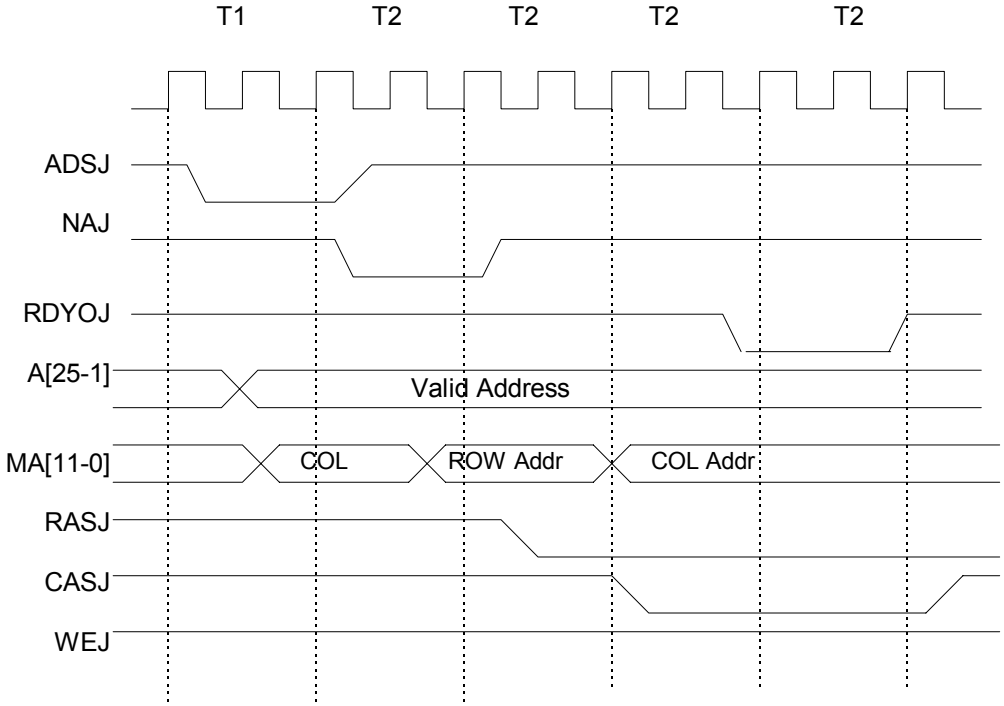
MA Table (continued)

DRAM mode	DRAM type	Bank	DRAM addr	MA0 MA1 MA2	MA3 MA4 MA5	MA6 MA7 MA8	MA9 MA10 MA11	Enable Bank
21	1M	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	
	4M	1,2	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 A10 A11	A12
22	1M	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 A10	
	4M	1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	
	4M	2,3	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 A10 A11	A12
23	2M	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA21 A10	
24	2M	0,1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10	A11
25	2M	0,1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10	A11
	4M	2,3	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 A10 A11	A12
26	2M	0	row column	A11 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA21 A10	
	4M	1	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	
27	4M	0	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	
28	4M	0,1	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 A10 A11	A12
29	4M	0,1	row column	PA21 PA22 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA23 A10 A11	A12
	4M	2	row column	PA21 A12 A13 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA22 A10 A11	
30	4M	0-3	row column	PA21 PA22 PA23 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA24 A10 A11	A13, A12
31	16M	0,1	row column	PA21 PA22 PA23 A2 A3 A4	A14 A15 A16 A5 A6 A7	PA17 PA18 PA19 A8 A9 A1	PA20 PA24 PA25 A10 A11 A12	A13

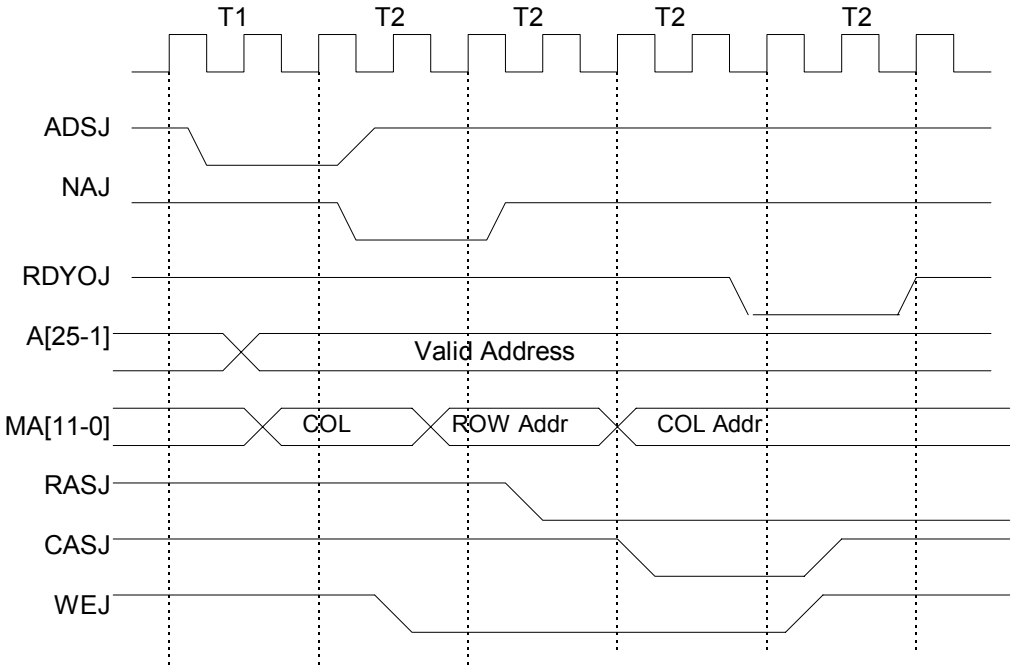
Refresh Address (RAS only)	RA2 RA3 RA4 RA5 RA6 RA7 RA0 RA1 RA8 RA9 RA10

Section 6 : Timing Diagrams

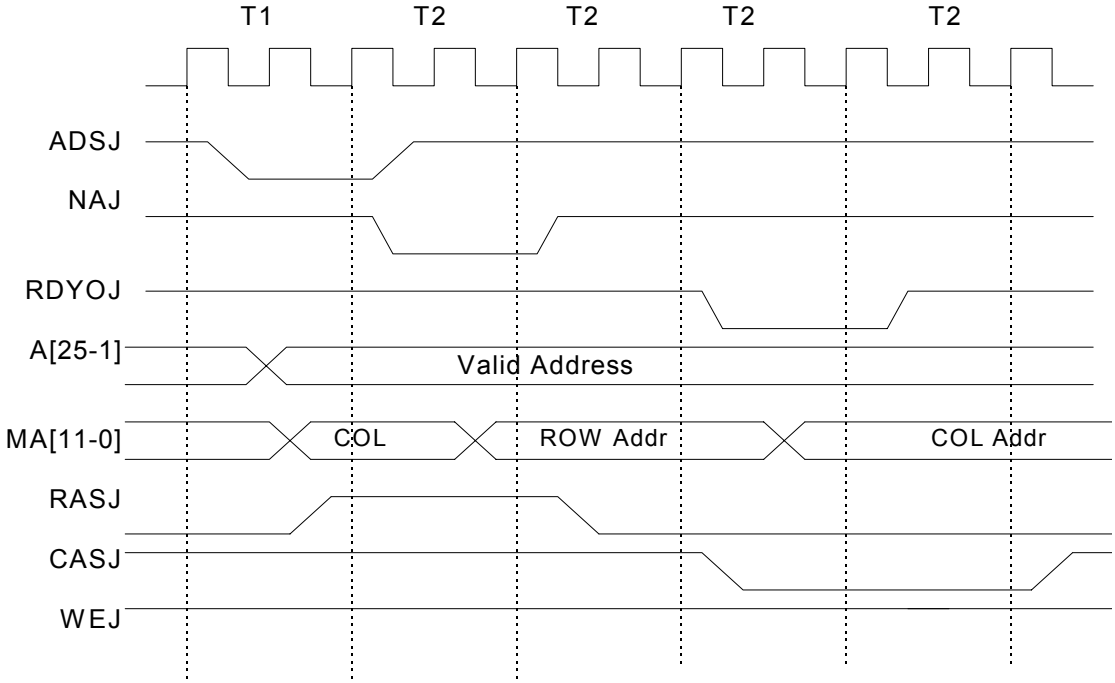
(A) **P9 Non-pipelined Read... Inactive .... 3 waits**



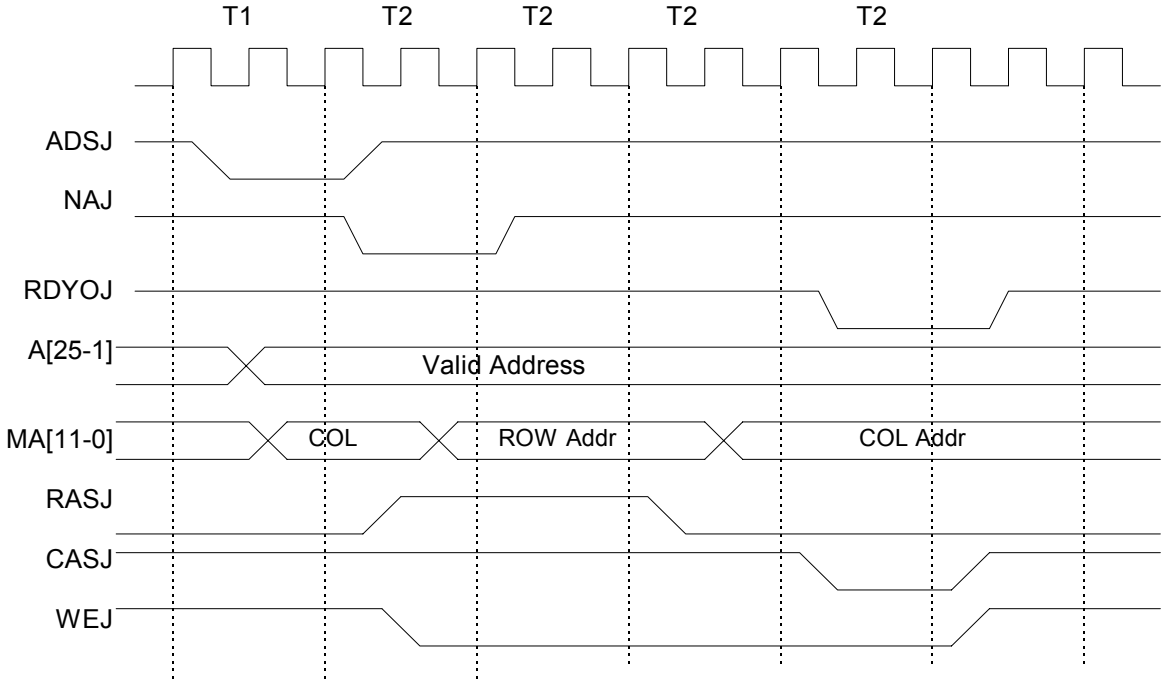
(B) **P9 Non-pipelined Write... Inactive .... 2 waits**



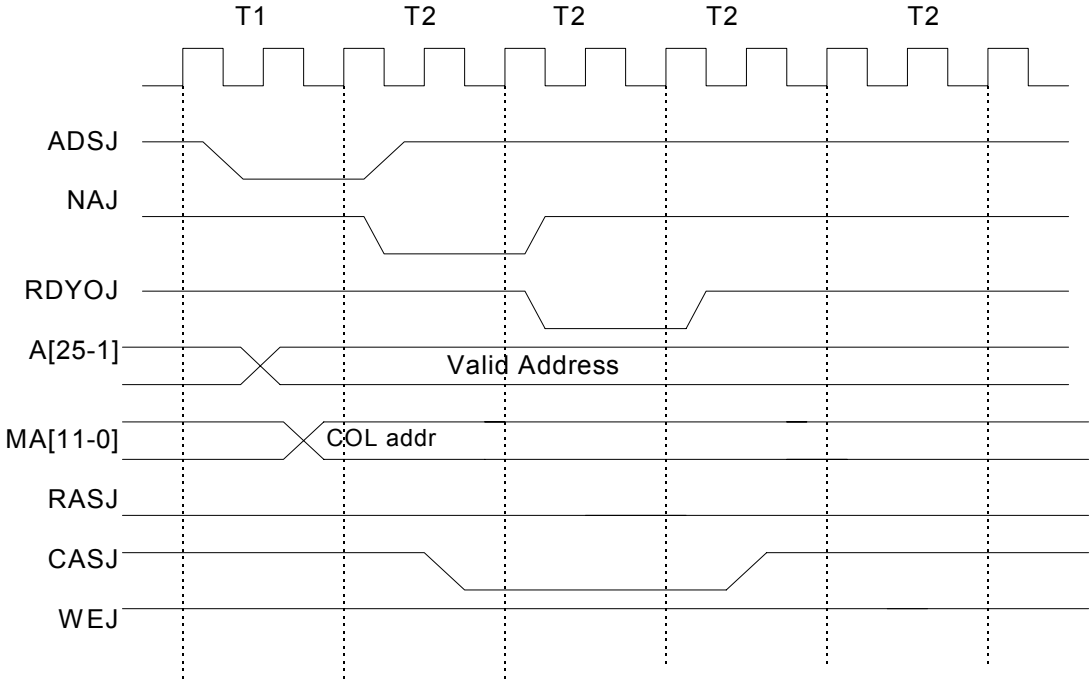
(C) **P9 Non-pipelined Read... Miss .... 4 waits**



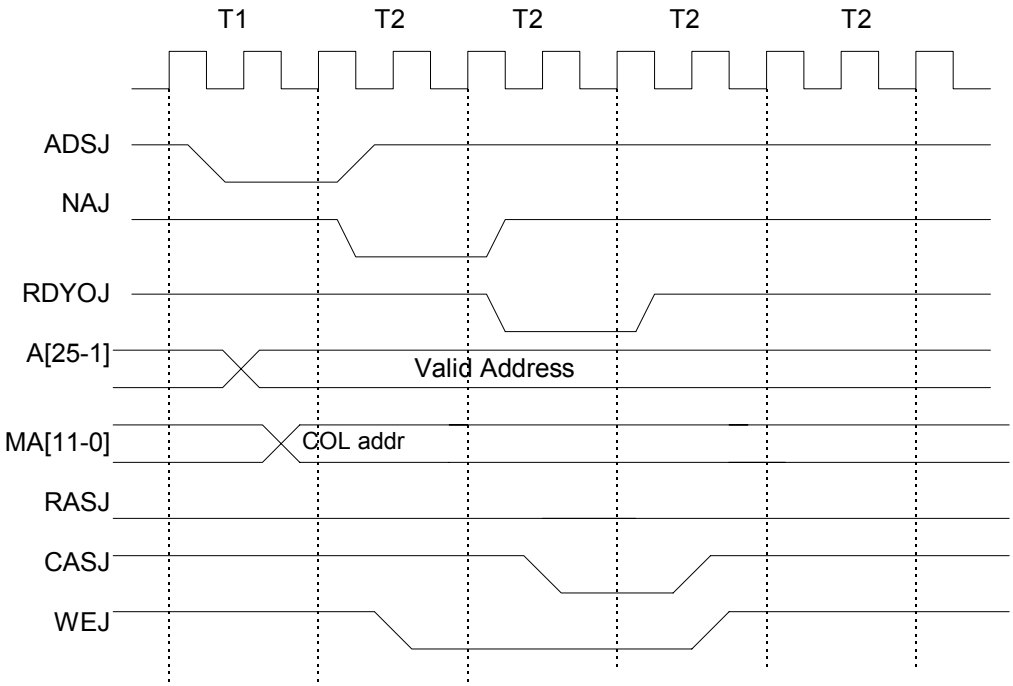
(D) **P9 Non-pipelined Write... Miss .... 3 waits**



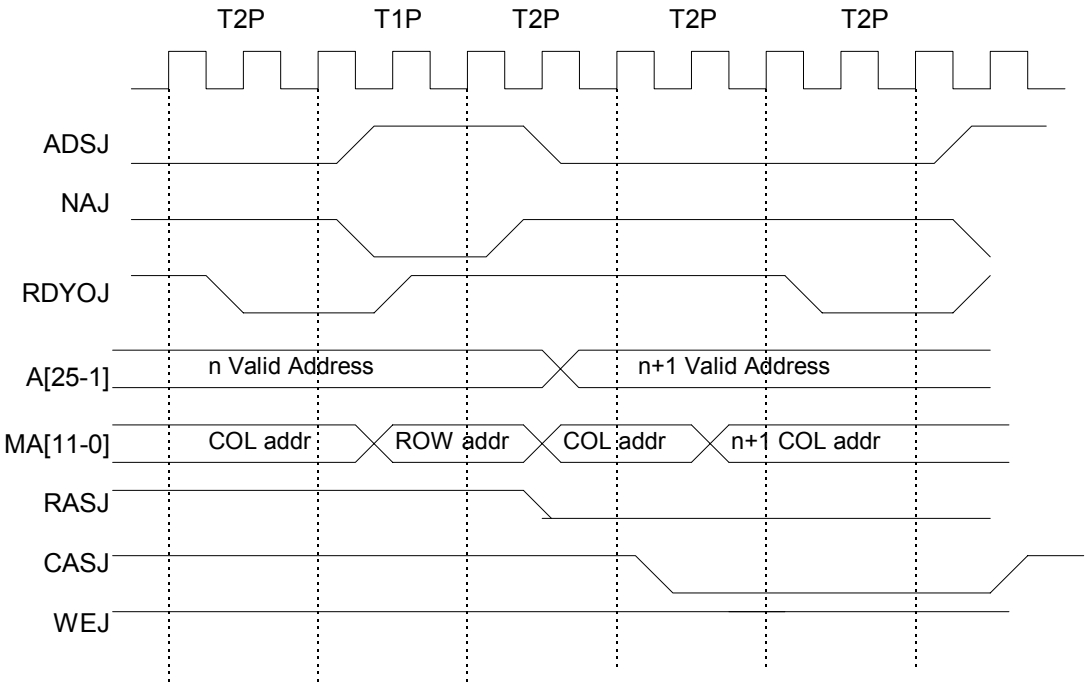
(E) **P9 Non-pipelined Read... Hit .... 1 wait**



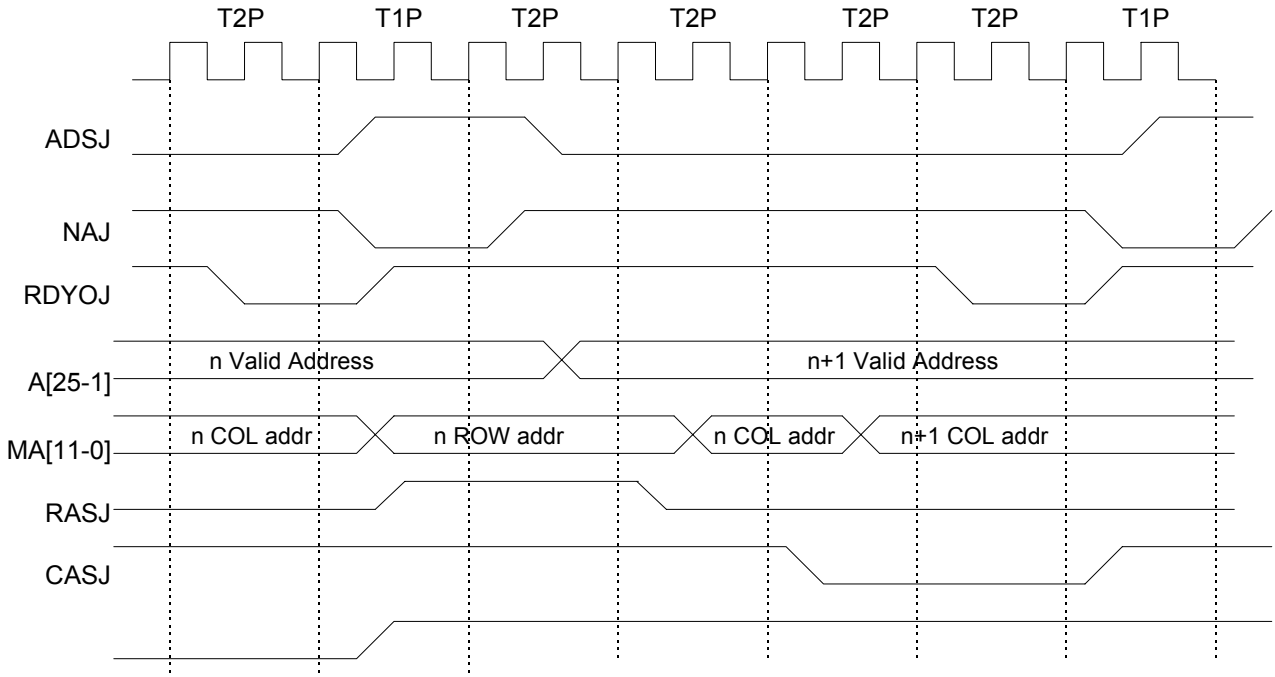
(F) **P9 Non-pipelined Write... Hit .... 1 wait**



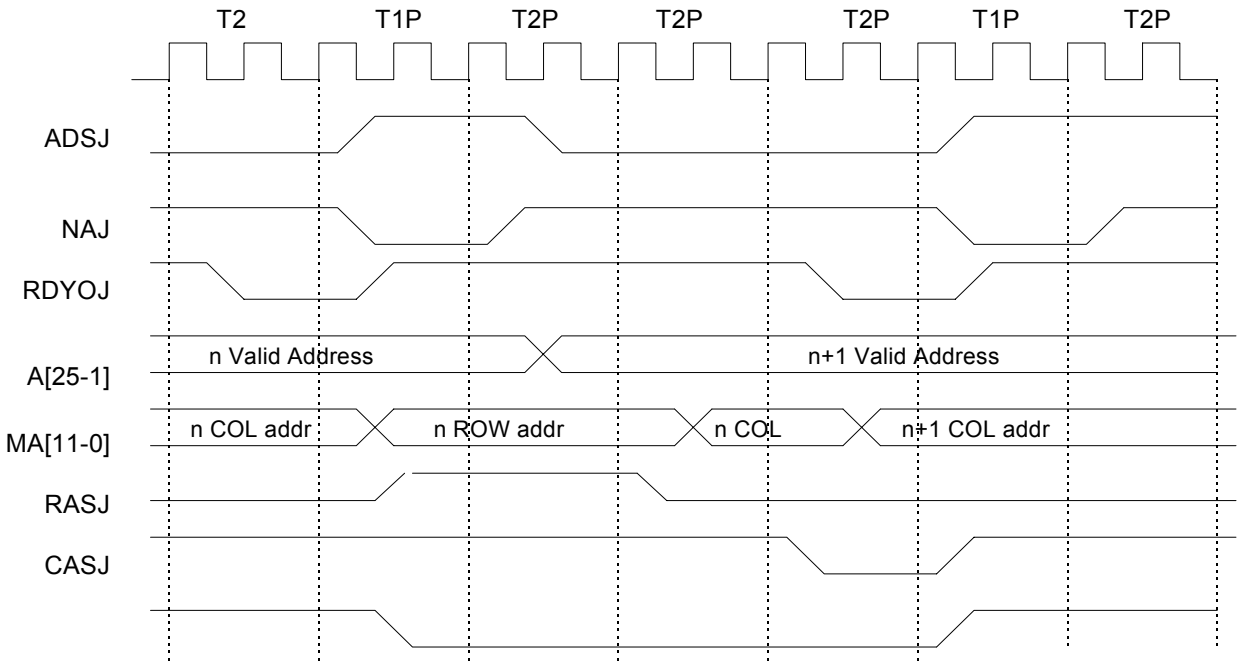
(G) **P9 Pipelined Read... Inactive .... 2 waits**



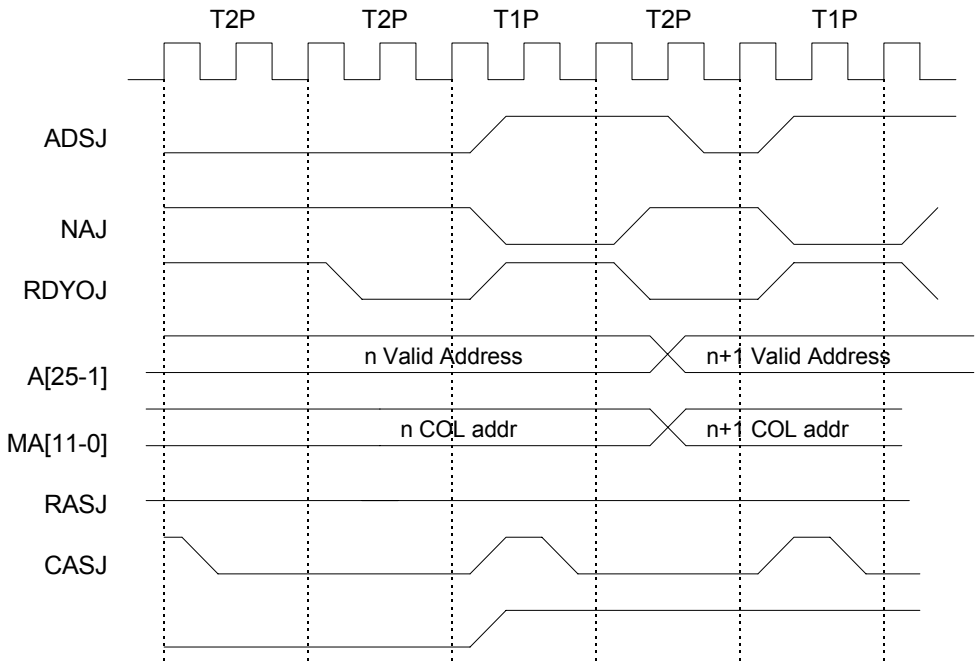
(H) **P9 Pipelined Read... Miss .... 3 waits**



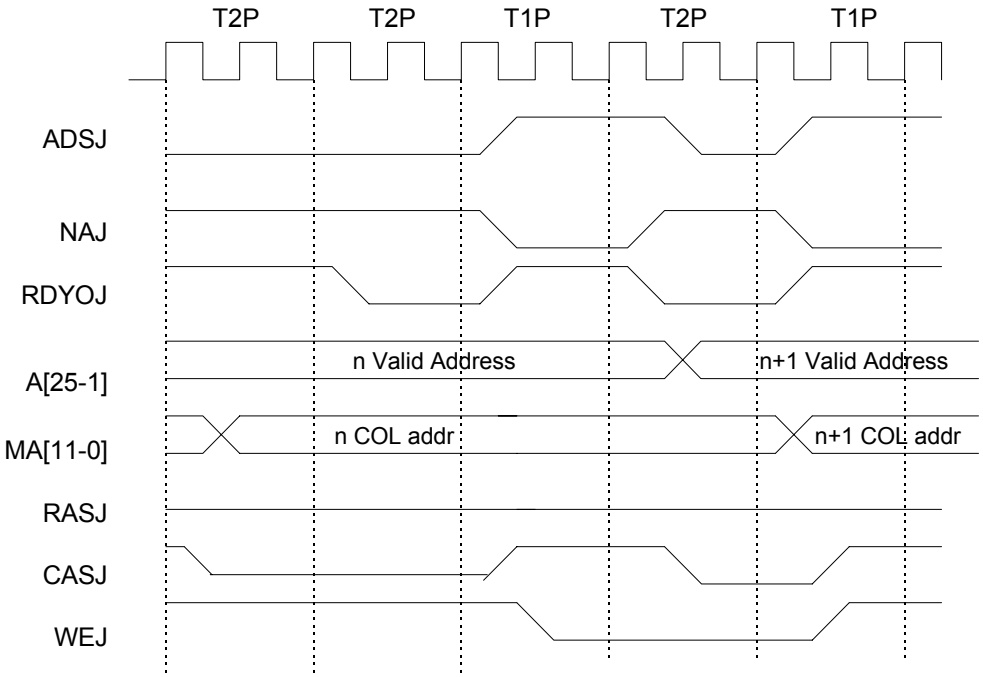
(I) **P9 Pipelined Write... Miss .... 2 waits**



(J) **P9 Pipelined Read... Hit .... 0 wait**



(K) **P9 Pipelined Write... Without Fast Write Hit .... 0 wait**



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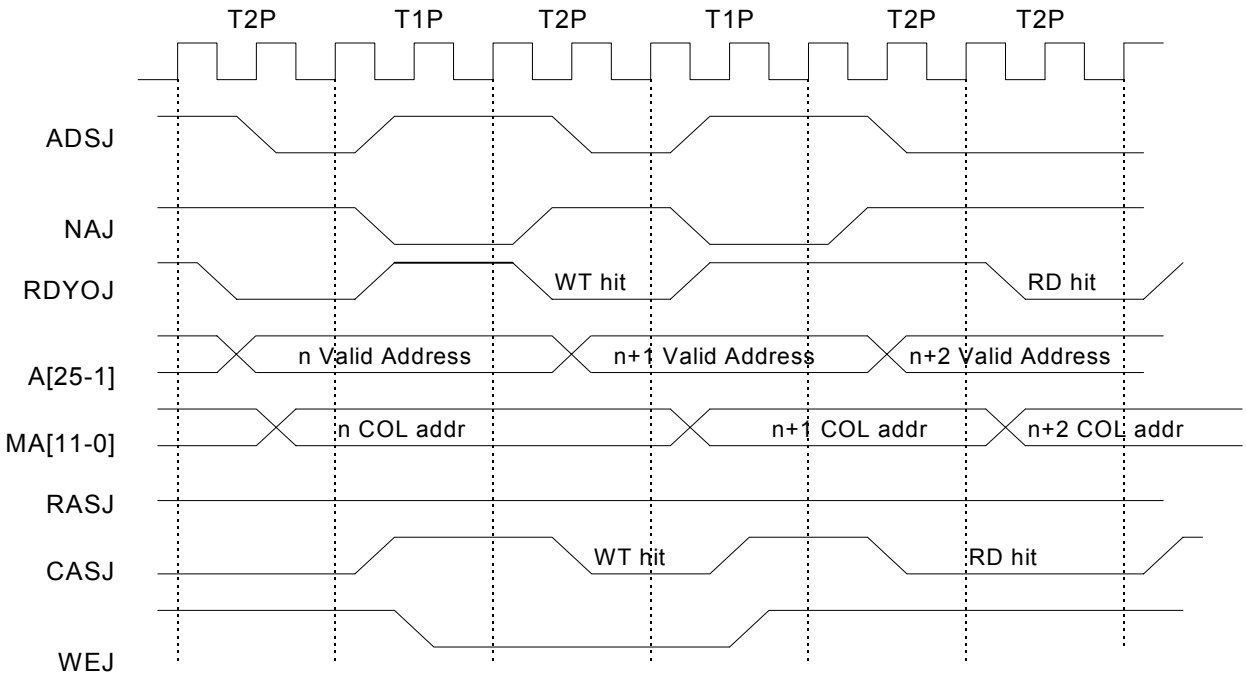
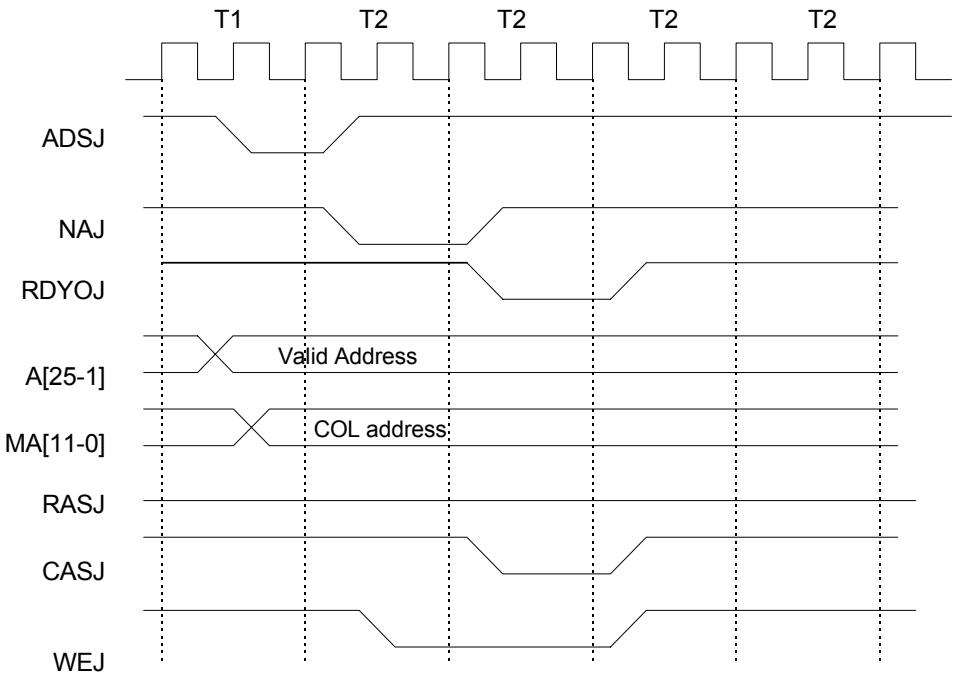
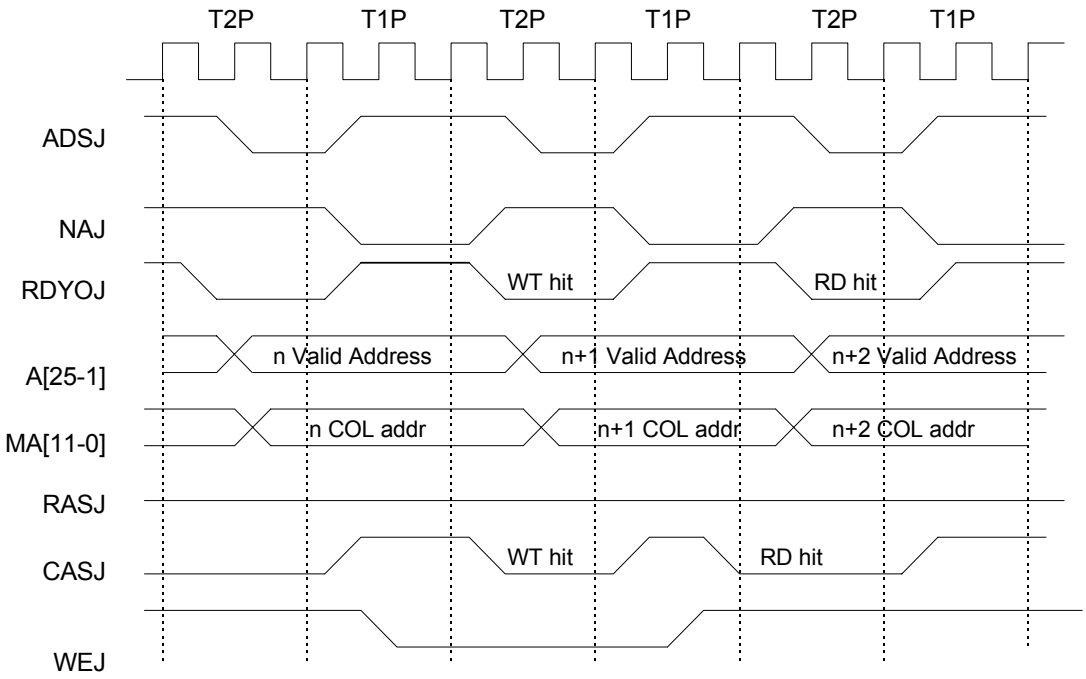
(L) **P9 Pipelined Read Hit after Write Hit... Add 1 wait**



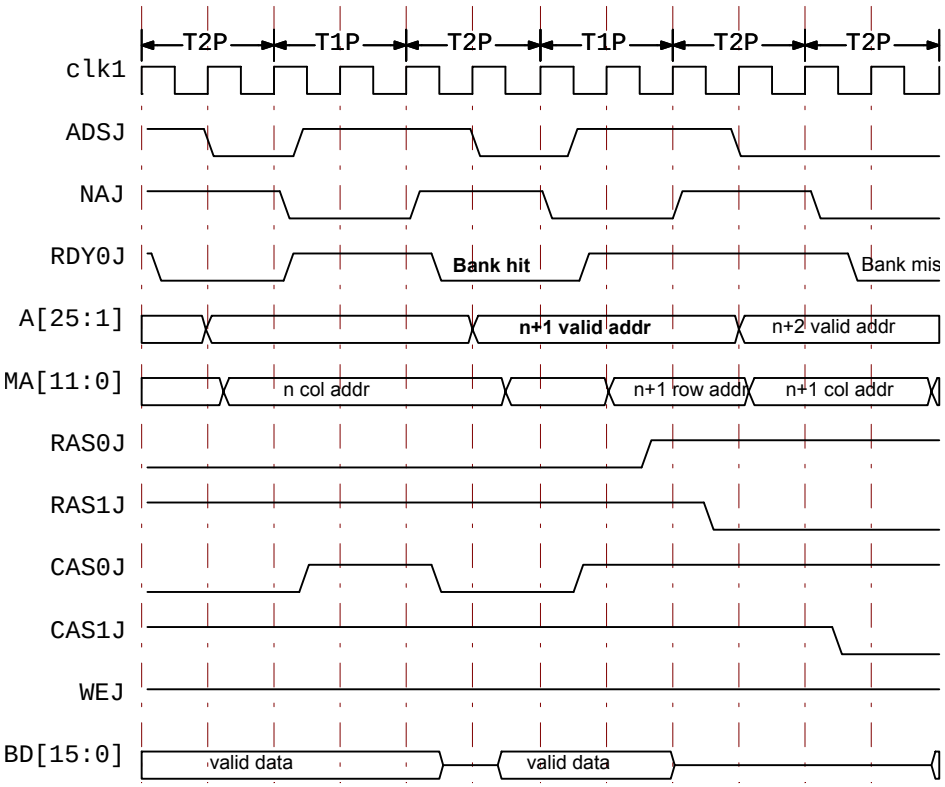
(M) **P9 Pipelined Write Hit... with Fast Write Hit... 1 wait**



(N) **P9 Pipelined Read Hit after Fast Write Hit... 0 wait**



(O) **Bank Miss for EDO DRAM Timing**



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Section 7 : Electrical Characteristics

7.1 Absolute Maximum Ratings

Although all inputs are protected against ESD or inadvertent connection to high voltages, exposure to stresses exceeding absolute maximum ratings may permanently damage the device or seriously affect reliability.

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	- 0.5	+ 7.0	V
Input Voltage	V_{IN}	- 0.5	Vcc + 0.5	V
Operating Temperature	T_{case}	0	+ 70	^oC
Storage Temperature	T_{Stg}	- 65	+ 100	^oC

7.2 D.C. Characteristics

Functional operating range: Tcase = 0 ºC ~ + 70 ºC
Vcc = 5V ± 5% 40 MHz / 5V

Parameter	Symbol	Min.	Max.	Unit	Note
Input Low Voltage	V_{IL}	- 0.3	+ 0.8	V	
Input High Voltage	V_{IH}	2.0	Vcc+0.3	V	
BCLK2 Input Low Voltage	V_{ILC}	- 0.3	+ 0.8	V	
BCLK2 Input High Voltage	V_{IHC}	Vcc-0.8	Vcc+0.3	V	
Output Low Voltage	V_{OL}	-	0.45	V	
Output High Voltage	V_{OH}	2.4	-	V	
Input Leakage Current	I_{LI}	-	±15	•	$0 V \le V_{IN} \le Vcc$
Input Pull Up Current	I_{LU}	-	- 250	•	V_{IL} = 0.45V
Input Pull Down Current	I_{LD}	-	- 250	•	V_{IH} = 2.4V
Output Leakage Current	I_{LO}	-	±15	•	
Power Supply Current	I_{CC}	-	290	mA	CLKT = 80 MHz
Power Save Mode	I_{PS}		50	mA	CLKT = 80 MHz

7.3 AC Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Notes
t_D	Data Flow from BD to SD delay		18	ns	Note 4
t_D	Data Flow from SD to BD delay		16	ns	Note 4
t_{VD}	16-bit MWTJ, MRDJ valid delay	112		ns	AT timing
t_{FD}	16-bit MWTJ, MRDJ float delay	9	18	ns	AT timing
t_{VD}	IDRJ, IDWJ, SMEMRJ, SMEMWJ valid delay	49		ns	AT timing
t_{FD}	IDRJ, IDWJ, SMEMRJ, SMEMWJ float delay	9	18	ns	AT timing
t_S	IO16J Input setup time	10		ns	AT timing
t_h	IO16J Input hold time	5		ns	AT timing
t_S	MEM16J Input setup time	10		ns	AT timing
t_h	MEM16J Input hold time	5		ns	AT timing
t_S	IOCHRDY Input setup time	15		ns	AT timing
t_h	IOCHRDY Input hold time	5		ns	AT timing
t_S	NOWSJ, MASTERJ Setup time	15		ns	AT timing
t_h	NOWSJ, MASTERJ Hold time	5		ns	AT timing
t_{VD}	BALE Valid delay	54		ns	AT timing
t_{FD}	BALE Float delay	3	7	ns	AT timing
t_S	REFRESHJ Input setup time	15		ns	AT timing
t_h	REFRESHJ Input hold time	5		ns	AT timing
t_{VD}	REFRESHJ Output valid delay	35		ns	AT timing
t_{FD}	REFRESHJ Output float delay	4	8	ns	AT timing
t_{VD}	ROMKBCSJ Valid delay	48		ns	Note 3
t_{FD}	ROMKBCSJ Float delay	33	40	ns	Note 3
t_S	IOCHKJ Input setup time	15		ns	AT timing
t_h	IOCHKJ Input Hold time	5		ns	AT timing
t_{VD}	RTCRJ, RTCWJ Valid delay			ns	Note 3
t_{FD}	RTCRJ, RTCWJ Float delay			ns	Note 3
t_S	IRQ Group Setup time	15		ns	AT timing
t_h	IRQ Group Hold time	5		ns	AT timing
t_S	DRQ Group Setup time	15		ns	AT timing
t_h	DRQ Group Hold time	5		ns	AT timing

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AC Characteristics (continued)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
	BCLK2		80	MHz	Clock signal
t_{VD}	BA2, BA23, BA24, BA25, BEHJ, BELJ, ADSJ, MIOJ, DCJ, WRJ, valid delay		10	ns	NP timing
t_{FD}	BA2, BA23, BA24, BA25, BEHJ, BELJ, ADSJ, MIOJ, DCJ, WRJ, float delay		10	ns	NP timing
t_S	BD0-BD15 Input setup time	5		ns	NP timing
t_h	BD0-BD15 Input hold time	3		ns	NP timing
t_{VD}	BD0-BD15 Output valid delay	20		ns	NP timing
t_{FD}	BD0-BD15 Output float delay	11		ns	NP timing
t_{VD}	RAS[3-0]J Valid delay	15		ns	DRAM timing
t_{FD}	RAS[3-0]J Float delay	5	11	ns	DRAM timing
t_{VD}	CAS[3-0][HL]J Valid delay	16		ns	DRAM timing
t_{FD}	CAS[3-0][HL]J Float delay	3	8	ns	DRAM timing
t_{VD}	MA[11-0] Valid delay	6		ns	DRAM timing
t_{FD}	MA[11-0] Float delay	3		ns	DRAM timing
t_{VD}	WEJ Valid delay	3		ns	DRAM timing
t_{FD}	WEJ Float delay	3	8	ns	DRAM timing
t_S	SA0, BHEJ Input setup time	4		ns	Note 3
t_h	SA0, BHEJ Input hold time	2		ns	Note 3
t_{VD}	SA[19,0], BHEJ Output Valid delay		2	ns	Note 3
t_{FD}	SA[19,0], BHEJ Output Float delay		8	ns	Note 3
t_{VD}	SD[15-0] Output Valid delay	0		ns	CPU timing
t_{FD}	SD[15-0] Output Float delay	3		ns	CPU timing
t_{VD}	DACKJ Group Valid delay	90		ns	AT timing
t_{FD}	DACKJ Group Float delay	15		ns	AT timing
t_{VD}	RSTDRV Valid delay	5		ns	CPU timing
t_{FD}	RSTDRV Float delay	4		ns	CPU timing
t_{skew1}	Time skew between ATCLK and BCLK2	9	20	ns	
t_{skew2}	Time skew between CK7M and OSC14M	6	12	ns	

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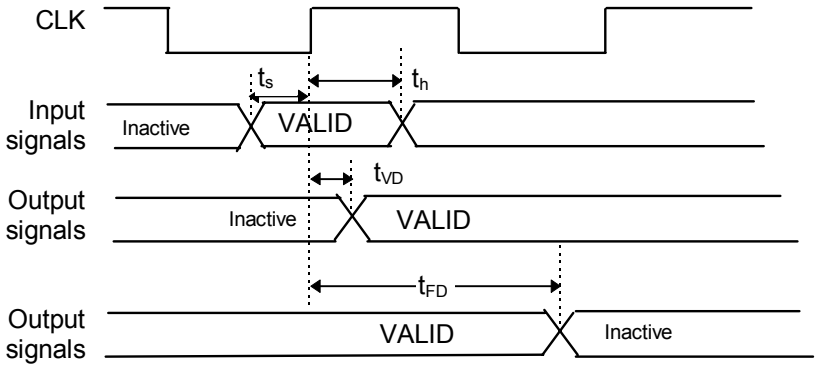
Meaning of symbols :

T_D	Data Flow delay
T_S	Input Setup time
T_h	Input Hold time
T_{VD}	Output Valid delay
T_{FD}	Output Float delay
T_{skew1}	Clock skew time between BCLK2 and ATCLK
T_{skew2}	Clock skew time between OSC14M and CK7M

Notes :

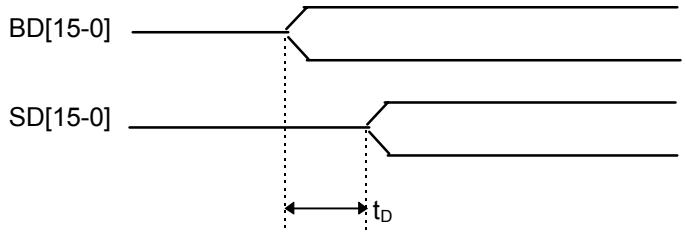
1. Parity data is only recognized in non-CPU memory read cycles, the timing requirements are related to command ending.
2. Parity data are only generated in non-CPU memory write cycles, the timing are related to the stable ISA data. The memory cycles in notes 2 and 3 refer to the on-board local memory cycles.
3. The timing refers to the generated delay after the CPU stable address.
4. The timing refers to propagating delay from BD to SD.
5. The timing refers to propagating delay from SD to BD.

The following pages show the input waveforms :
Setup, Hold, Valid, Float Delay time description

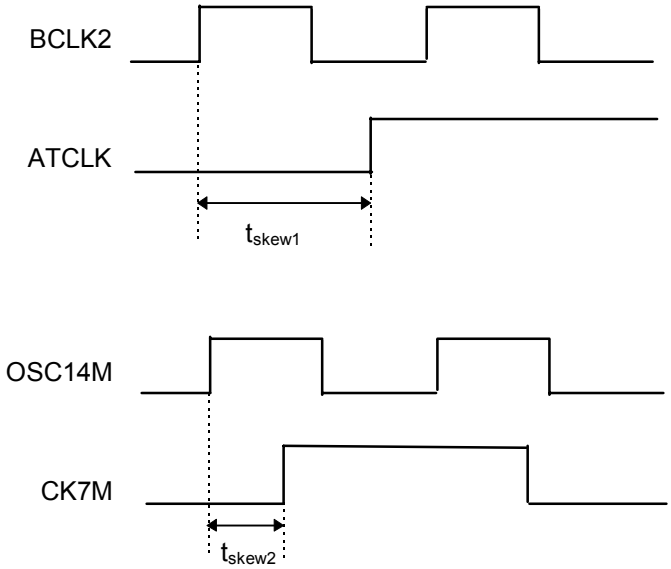


Note : 1. For coprocessor and DRAM side signals, CLK = CLK2
2. For ISA side signals, CLK = ATCLK
3. Signal reference level = 1.5 V
4. Environment : loading 50 pF

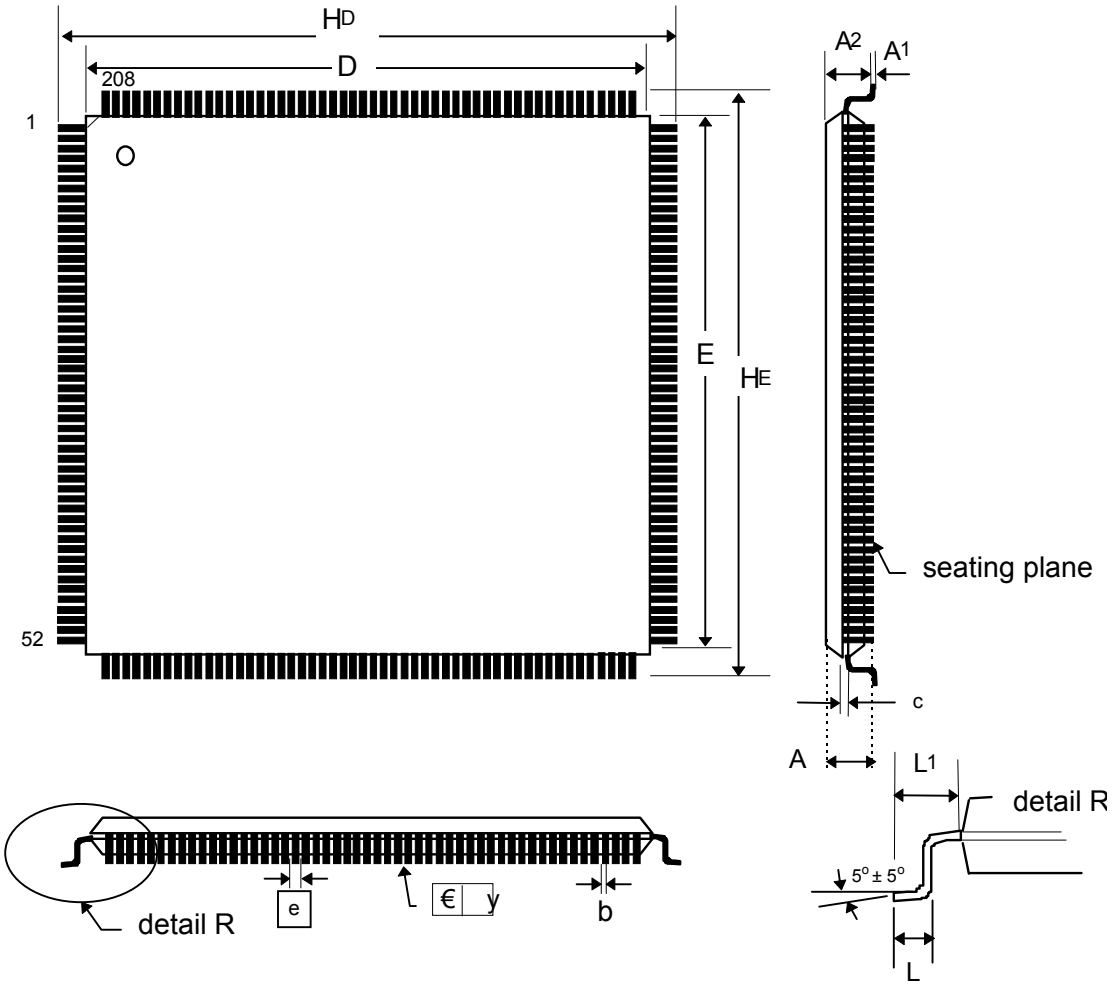
Data Flow Delay Description



Clock Skew Time Description



Section 8 : Packaging Information



Symbol	Dimensions in Millimeters (nom)	Dimensions in Inches (nom.)
A	3.5 (max)	0.137 (max)
A_1	0.2 (min)	0.008 (min)
A_2	3.0	0.118
b	0.18	0.007
c	0.15	0.006
D	28.0	1.102
E	28.0	1.102
e	0.5	0.020
H_D	30.6	1.205
H_E	30.6	1.205
L_1	1.3	0.051
L	0.5	0.020
y	0.15 (max)	0.006 (max)

Appendix

Subject : **New Improvement of Power Good Circuit on M6117**
Date : **October 1, 1997**
Part & Version : **Total Pages : 4**

To : **All Distributors & M6117 Customers**
From : **Fencer J.A. Chen Ext. 5128 / Ali , email: jachen@ali.com.tw**

Note : M6117 needs delay of 150ms for PWG signal.

0. Please refer to Fig.1 for PWG circuit.

1. PWG form power supply:

- Power good delay time depends on the power supply spec.
- PWG rise time depends on R8 / C2 value, warm reset delay time depends on C2 / R9 value.
- Please refer to Fig.2 - Fig. 4 for scope timing.

2. PWG form LM393

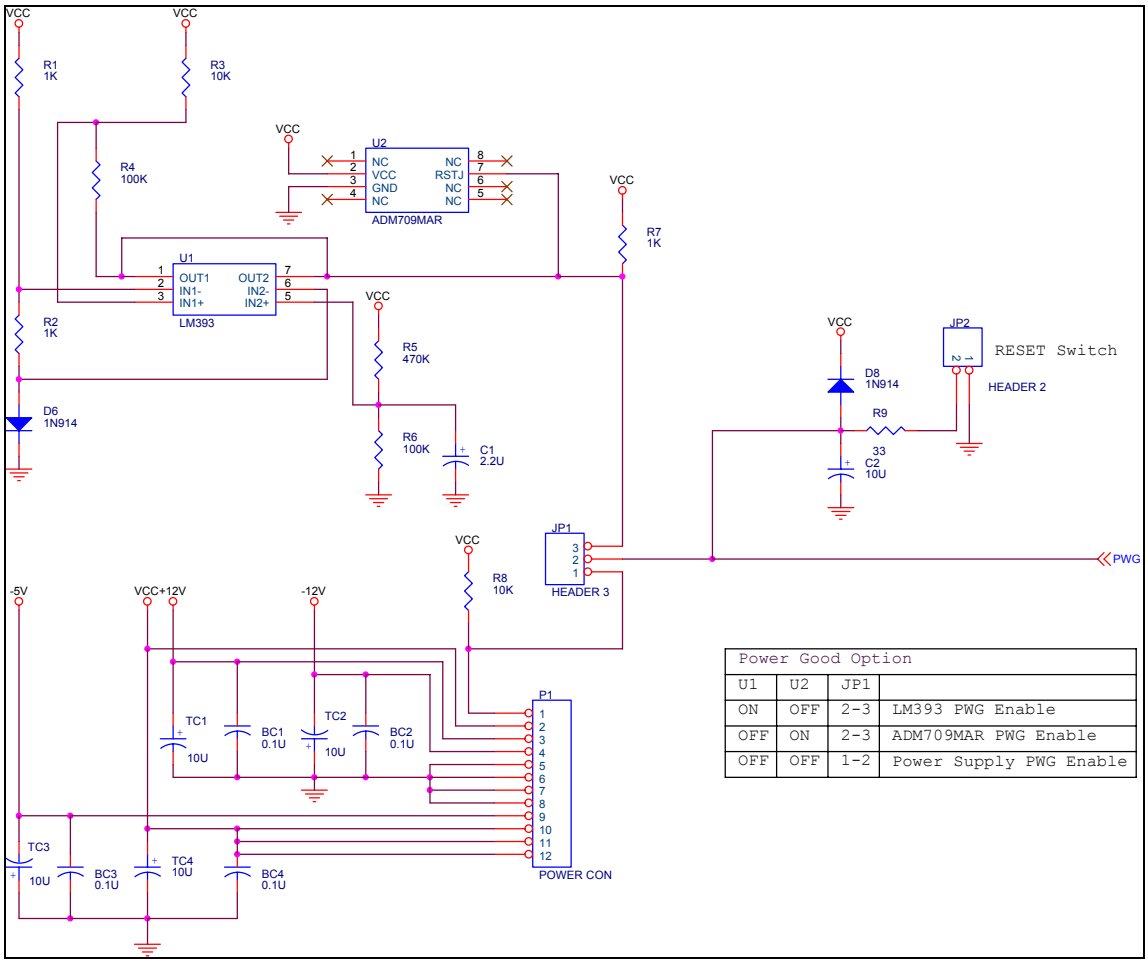
- PWG rise time, delay time, warm reset delay time all depend on R / C value.
- PWG delay time depends on R5,R6 / C1 value (see table1 for delay time setting), PWG rise time depends on R7 / C2 value, warm reset delay time depends on C2 & R9 value.
- Please ***add C1*** for LM393 circuit and modify R5 & R6 to 470K & 100K. If we do not modify LM393 circuit for PWG, there may be some power-on failure on high speed application (such as 40Mhz). This change will insert delay time for VCC rise to valid voltage.
- Please refer to Fig.5 - Fig. 9 for scope timing.

R5	R6	C1	Delay Time
470K	100K	10U	1080ms
470K	100K	4.7U	350ms
470K	100K	2.2U	306ms
47K	10K	10U	150ms
47K	10K	4.7U	98ms

Table1 LM393 delay time

3. PWG form ADM709MAR

- PWG delay time fix in 184 ms by ADI.
- PWG rise time depends on R7 / C2 value, warm reset delay time depends on C2 / R9 value.
- Please refer to Fig.10 - Fig. 12 for scope timing.



Power Good Option			
U1	U2	JP1	
ON	OFF	2-3	LM393 PWG Enable
OFF	ON	2-3	ADM709MAR PWG Enable
OFF	OFF	1-2	Power Supply PWG Enable

Fig.1 Power good circuit

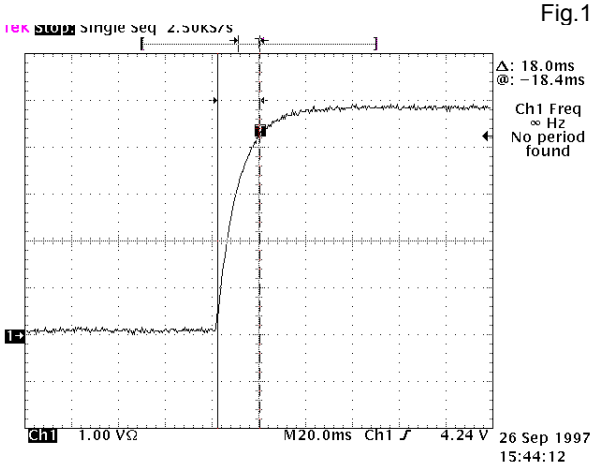


Fig.2 Power supply PWG rise(18ms)

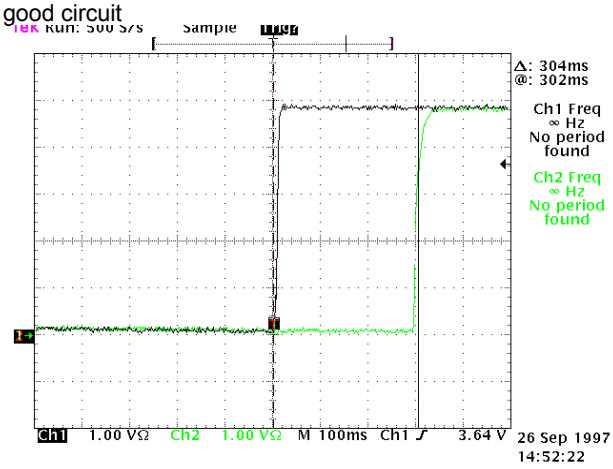


Fig.3 Power supply PWG delay time(304ms)

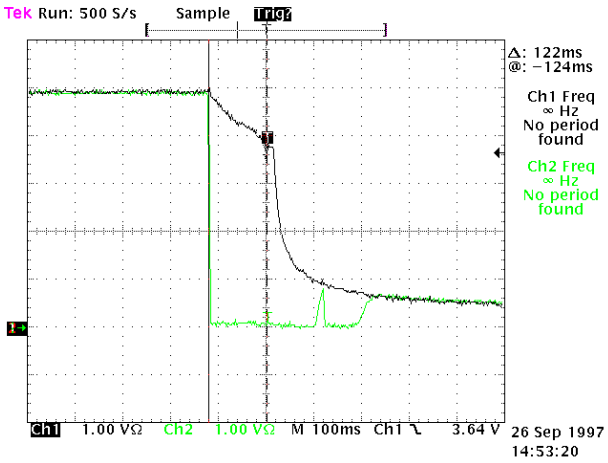


Fig.4 Power supply Power Fail Delay time(122ms)

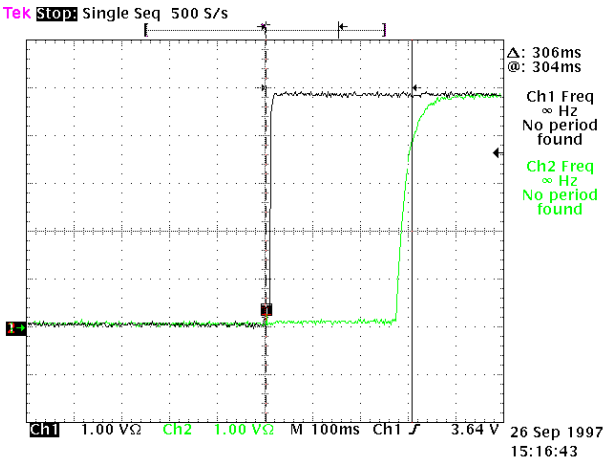


Fig.5 LM393 PWG delay time (org. , no delay)

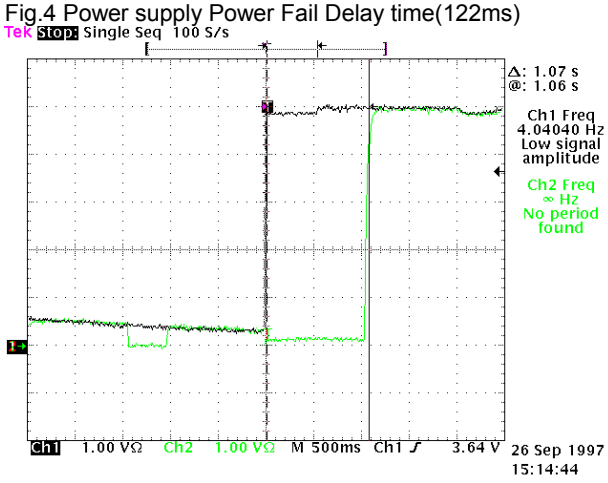


Fig.6 LM393 PWG Delay time(1.07s by 10U)

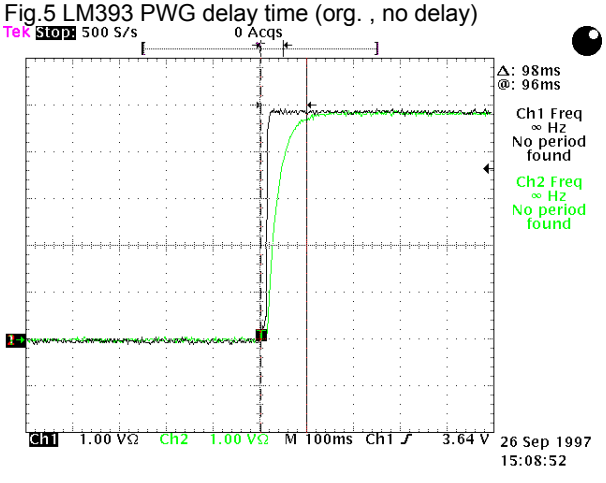


Fig.7 LM393 PWG Delay time(306ms by 2.2U)

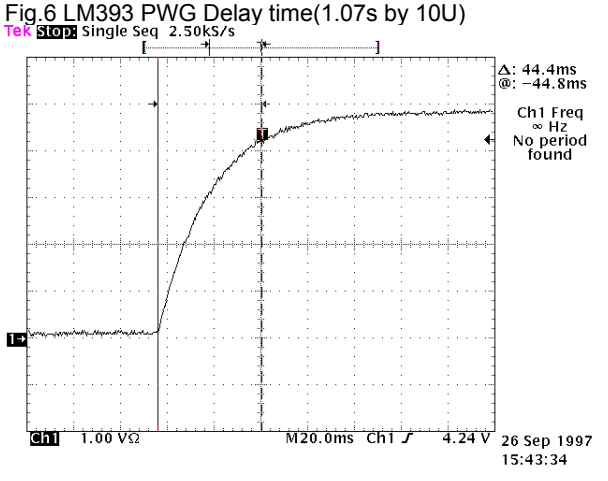


Fig.8 LM393 PWG rise(44.4ms)

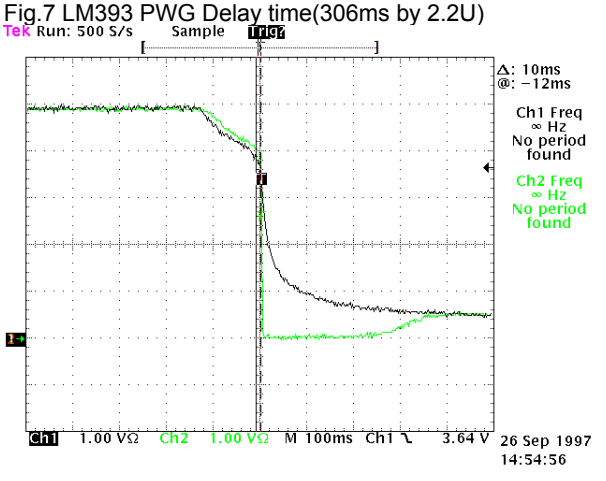


Fig.9 LM393 PF Delay time(0ms)

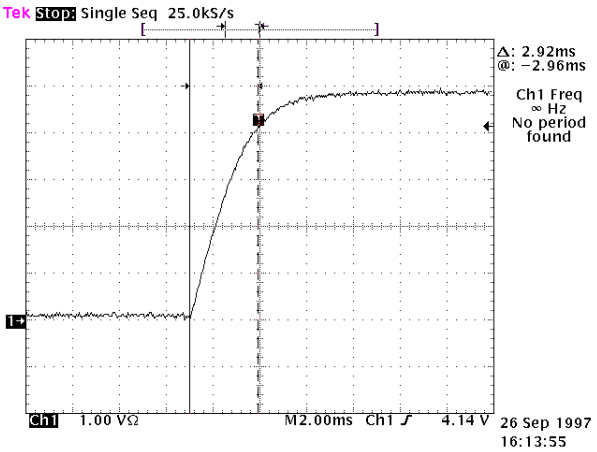


Fig.10 ADM709 PWG rise(2.92ms)

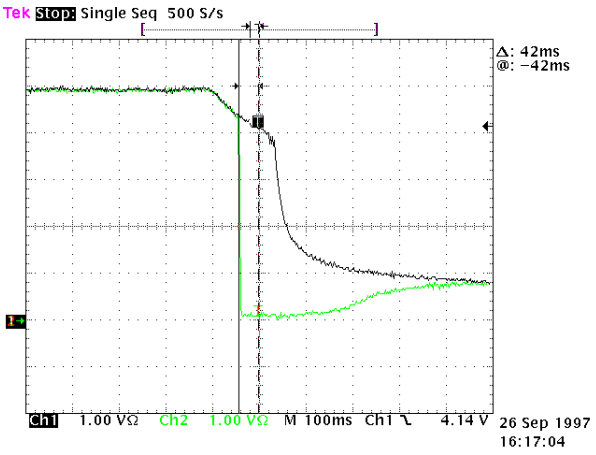


Fig.11 ADM709 Power Fail delay time(42ms)

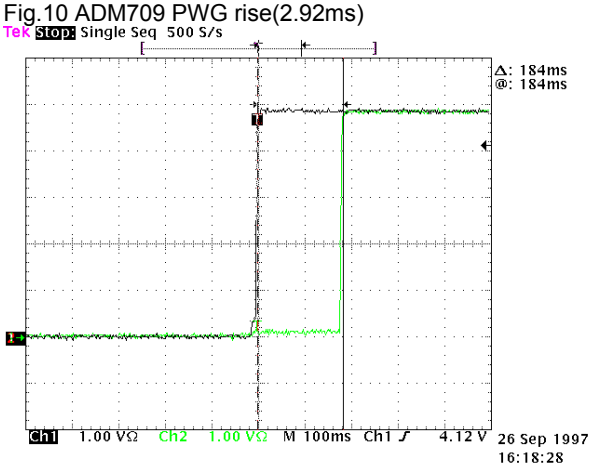


Fig.12 ADM709 PWG delay time(184ms)

Example A: Set timeout 16 sec to generate a system reset.

; Please use TASM to compiler the following program.
; Execute under DOS environment.

Reset watchdog timer

Resets the watchdog timer periodically to prevent timeout.

8F-1,No.22,Wuchyuan 2RD.,Hsin Chuang city Taipei Hsien, Taiwan, R.O.C. Tel: 886-(02) 2298-0770 Fax: (02) 2299-1883

```
;
.286
.model small
.code
Start proc c
      mov ax,0c513h   ; Unlock config register
      call writechip
      mov ax,3737h    ; Disable watchdog timer
      call readchip
      and al,10111111b
      xchg ah,al
      call writechip
      mov ax,083bh    ; Set the expected counter value
      call writechip     ; to [080000h]
      mov ax,003ah    ; 30.5usec * 080000h = 16 sec
      call writechip
      mov ax,0039h
      call writechip
      mov ax,3838h    ; Select "System reset" as timeout actiom
      call readchip
      and al,00001111b
      or al,11010000b
      xchg ah,al
      call writechip
      mov ax,3737h    ; Enable watchdog timer
      call readchip
      or al,01000000b
      xchg ah,al
      call writechip
      mov ax,0013h    ; Lock config register
      call writechip
      mov ax,4c00h
      int 21h
      endp

readchip proc c
      out 22h,al
      nop
      nop
      in al,23h
      nop
      nop
      ret
      endp

writechip proc c
      out 22h,al
      nop
      nop
      xchg ah,al
      out 23h,al
      nop
      nop
      xchg ah,al
      ret
      endp
end
```

```
      mov ax,0c513h  ;Unlock configuration register
      call writechip
      mov ax,3c3ch    ; reset watchdog timer counter
      call readchip
      or al,01000000b; The counter is reset at out 23h,al
      xchg ah,al
      call writechip
      mov ax,0013h    ; Lock configuration register
      call writechip
```

(the above code uses reachip and writechip procedures)

Example B: Set GPCS0 decoder to I/O address 100h, 101h 8bit data bus write only.

```
; Please use TASM to compiler the following program.
; Execute under DOS environment.
;
.286
.model small
```

```
.code
Start proc c
      mov ax,0c513h   ; Unlock configuration register
      call writechip
      mov ax,0444h    ; Enable IO address A[15-1], 8bit data bus write only.
      call writechip
      mov ax,0141h    ; Set the GPCS0 A[15-8] is 01h.  A15  A14  A13  A12  A11  A10  A9  A8  A7  A6  A5  A4  A3  A2  A1  A0
      call writechip  ;                                0    0    0    0    0    0    0   1   0   0   0   0   0   0   0   X  = 100h, 101h
      mov ax,0040h    ; Set the GPCS0 A[7-1] is 00h.
      call writechip
      mov ax,0043h    ; Set the GPCS0 mask A[15-8] is 00h,  address A[15-8] full compare(set to" 0"  is compare, set to "1" is don't care).
      call writechip
      mov ax,0042h    ; Set the GPCS0 mask A[7-1] is 0000000Xb, address A[7-1] full compare.
      call readchip     :
      and al,00000001b
      or al,00000000b ;
      xchg ah,al      ;
      call writechip  ;
      mov ax,0040h    ;
      call readchip
      or al,00000001b
      xchg ah,al
      call writechip  ; Active GPCS0 decoder single.
      mov ax,0013h    ; Lock configuration register
      call writechip
      mov ax,4c00h
      int 21h
      endp

readchip proc c
      out 22h,al
      nop
      nop
      in al,23h
      nop
      nop
      ret
      endp

writechip proc c
      out 22h,al
      nop
      nop
      xchg ah,al
      out 23h,al
      nop
      nop
      xchg ah,al
      ret
      endp
end
```

Example C: Set GPCS1 decoder to I/O address 168h to16Bh 8bit data bus read/write.

```
; Please use TASM to compiler the following program.
; Execute under DOS environment.
;
.286
.model small
.code
Start proc c
      mov ax,0c513h   ; Unlock configuration  register
```

```
        call writechip
        mov ax,0c45h    ; Enable IO address A[15-1], 8bit data bus read/write.
        call writechip
        mov ax,0149h    ; Set the GPCS0 A[15-8] is 01h.  A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
        call writechip  ;                                0   0   0   0   0   0   0  1  0  1  1  0  1  0  X  X  = 168h - 16Bh
        mov ax,6848h    ; Set the GPCS0 A[7-1] is 68h.
        call writechip
        mov ax,004bh    ; Set the GPCS0 mask A[15-8] is 00h,  address A[15-8] full compare(set to" 0"  is compare, set to "1" is don't care).
        call writechip
        mov ax,004ah    ; Set the GPCS0 mask A[7-1] is 000000XXb, address A[7-2] full compare, A[1-0] is don't care.
        call readchip   :
        and al,00000001b
        or al,00000010b ;
        xchg ah,al      ;
        call writechip  ;
        mov ax,0048h    ;
        call readchip
        or al,00000001b
        xchg ah,al
        call writechip  ; Active GPCS1 decoder single.
        mov ax,0013h    ; Lock configuration register
        call writechip
        mov ax,4c00h
        int 21h
        endp

readchip proc c
        out 22h,al
        nop
        nop
        in al,23h
        nop
        nop
        ret
        endp

writechip proc c
        out 22h,al
        nop
        nop
        xchg ah,al
        out 23h,al
        nop
        nop
        xchg ah,al
        ret
        endp
end
```

Example D: Set GPCS0 decoder to Memory address C800:0 to C800:3FFF(16Kbyte) 8bit data bus read/write.

```
; Please use TASM to compiler the following program.
; Execute under DOS environment.
;
.286
.model small
.code
Start proc c
        mov ax,0c513h   ; Unlock configuration register
        call writechip
        mov ax,3144h    ; Enable memory address A[25-11], 8bit data bus read/write.
        call writechip
        mov ax,0341h    ; Set the GPCS0 A[25-18] is 03h.  A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10
```

```
        call writechip      ;                                   0   0   0   0   0   0   1   1   0   0   1   0   0   0   0   X
        mov ax,2040h    ; Set the GPCS0 A[17-11] is 20h.
        call writechip
        mov ax,0043h    ; Set the GPCS0 mask A[25-18] is 00h,  address A[25-18] full compare(set to" 0"  is compare, set to "1" is don't care).
        call writechip
        mov ax,0042h    ; Set the GPCS0 mask A[17-11] is 0000111Xb, address A[17-11] high nibble compare, low nibble don't care.
        call readchip     :
        and al,00000001b
        or al,00001111b ;  set low nibble is don't care compare.
        xchg ah,al        ;
        call writechip    ;
        mov ax,0040h      ;
        call readchip
        or al,00000001b
        xchg ah,al
        call writechip    ; Active GPCS0 decoder single.
        mov ax,0013h      ; Lock configuration register
        call writechip
        mov ax,4c00h
        int 21h
        endp

readchip proc c
        out 22h,al
        nop
        nop
        in al,23h
        nop
        nop
        ret
        endp

writechip proc c
        out 22h,al
        nop
        nop
        xchg ah,al
        out 23h,al
        nop
        nop
        xchg ah,al
        ret
        endp
end
```

Example E: Set GPIO[7-0] is output pin, GPIO[15-8] is input pin.

```
; Please use TASM to compiler the following program.
; Execute under DOS environment.
;
.286
.model small
.code
Start proc c
        mov ax,0c513h   ; Unlock configuration  register
        call writechip
        mov ax,0ff4eh     ; Enable GPIO[7-0] is output pin.
        call writechip
        mov ax,004fh      ; Set the GPIO[15-8] is input pin.
        call writechip      ;
```

```
        mov ax,5547h    ; Output data value is 55h to output pin GPIO[7-0].
        call writechip
        mov ax,004ah    ; Input data value from GPIO[15-8].
        call readchip   ;
        mov ax,0013h    ; Lock configuration register
        call writechip
        mov ax,4c00h
        int 21h
        endp

readchip proc c
        out 22h,al
        nop
        nop
        in al,23h
        nop
        nop
        ret
        endp

writechip proc c
        out 22h,al
        nop
        nop
        xchg ah,al
        out 23h,al
        nop
        nop
        xchg ah,al
        ret
        endp
end
```

Example F: How to check M6117D hardware version.

```
; Please use TASM to compiler the following program.
; Execute under DOS environment.
;
.286
.model small
.code
Start proc c
        mov ax,0c513h   ; Unlock configuration  register
        call writechip
        mov ax,0036h
        call readchip       ; Bit 2,1,0 =  010 b
        and al,00000111b
        cmp al,00000010b
        je setflag
        stc                 ; If Error return carry flag is 1.
        jmp exitdos
```

```
setflag:
      clc                ; if OK return carry flag is 0.
exitdos:
      mov ax,4c00h
      int 21h
      endp

readchip proc c
      out 22h,al
      nop
      nop
      in al,23h
      nop
      nop
      ret
      endp

writechip proc c
      out 22h,al
      nop
      nop
      xchg ah,al
      out 23h,al
      nop
      nop
      xchg ah,al
      ret
      endp
end
```

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