Pin Information for the Cyclone™ EP1C12 Device
Version 1.4

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B1	VREF0B1	IO	LVDS23p	INIT_DONE	1	D4	C3			
B1	VREF0B1	IO	LVDS23n	CRC_ERROR	2	C3	C2			
B1	VREF0B1	IO	LVDS22p	CLKUSR	3	C2	D3			
B1	VREF0B1	IO	LVDS22n		4	B1	D2			
B1	VREF0B1	IO	VREF0B1		5	G5	D4			
B1	VREF0B1	IO			6	F4	D1			
B1	VREF0B1	IO	LVDS21p		7	D3	E3	DQ0L0	DQ0L0	DQ0L0
B1	VREF0B1	IO	LVDS21n		8	E4	E2	DQ0L1	DQ0L1	DQ0L1
B1	VREF0B1	VCCIO1			9					
B1	VREF0B1	GND			10					
B1	VREF0B1	IO	DPCLK1		11	F5	F1	DQS0L	DQS0L	DQS0L
B1	VREF0B1	IO	LVDS20p		12	E3	E4	DQ0L2	DQ0L2	DQ0L2
B1	VREF0B1	IO	LVDS20n		13	D2	E5	DQ0L3	DQ0L3	DQ0L3
B1	VREF0B1	IO	LVDS19p		14	E2	F2			
B1	VREF0B1	IO	LVDS19n		15	D1	F3			
B1	VREF0B1	IO	LVDS18p		16	F3	F4			
B1	VREF0B1	IO	LVDS18n		17	G3	F5			
B1	VREF0B1	IO	LVDS17p		18	F2	G1			
B1	VREF0B1	IO	LVDS17n		19	E1	G2			
B1	VREF0B1	IO	LVDS16p		20	G2	F6			
B1	VREF0B1	IO	LVDS16n		21	F1	F7	DM0L	DM0L	
B1	VREF0B1	IO	LVDS15p				G3			
B1	VREF0B1	IO	LVDS15n				G4			DQ0L4
B1	VREF0B1	IO	LVDS14p				G5			DQ0L5
B1	VREF0B1	IO	LVDS14n				G6			DQ0L6
B1	VREF0B1	IO					H1			DQ0L7
B1	VREF0B1	VCCIO1			22					
B1	VREF0B1	GND								
B1	VREF1B1	IO	LVDS13p				H2			
B1	VREF1B1	IO	LVDS13n				H3			
B1	VREF1B1	IO	LVDS12p				H4			
B1	VREF1B1	IO	LVDS12n				H5			DM0L
B1	VREF1B1	IO	VREF1B1		23	H5	H6			
B1	VREF1B1	IO		nCSO	24	G4	J1			
B1	VREF1B1	DATA0		DATA0	25	H2	H7			
B1	VREF1B1	nCONFIG		nCONFIG	26	H3	J2			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
	VREF1B1	VCCA_PLL1			27	H6	J5			
B1	VREF1B1	CLK0	LVDSCLK1p		28	G1	J3			
B1	VREF1B1	CLK1	LVDSCLK1n		29	H1	J4			
	VREF1B1	GNDA_PLL1			30	J6	K1			
	VREF1B1	GNDG_PLL1			31	J5	J6			
B1	VREF1B1	nCEO		nCEO	32	H4	K2			
B1	VREF1B1	nCE		nCE	33	J4	J7			
B1	VREF1B1	MSEL0		MSEL0	34	J3	K3			
B1	VREF1B1	MSEL1		MSEL1	35	J2	K7			
B1	VREF1B1	DCLK		DCLK	36	K4	L1			
B1	VREF1B1	IO		ASDO	37	K3	K6			
B1	VREF1B1	IO	PLL1_OUTp		38	J1	K4			
B1	VREF1B1	IO	PLL1_OUTn		39	K2	K5			
B1	VREF1B1	IO	LVDS11p				L7			DM1L
B1	VREF1B1	IO	LVDS11n				L6			
B1	VREF1B1	IO	LVDS10p				L2			
B1	VREF1B1	IO	LVDS10n				L3			
B1	VREF1B1	IO	LVDS9p				L5			
B1	VREF1B1	IO	LVDS9n				L4			
B1	VREF2B1	VCCIO1								
B1	VREF2B1	GND			40					
B1	VREF2B1	IO					M1			DQ1L0
B1	VREF2B1	IO	LVDS8p				M3			DQ1L1
B1	VREF2B1	IO	LVDS8n				M2			DQ1L2
B1	VREF2B1	IO	LVDS7p				M5			DQ1L3
B1	VREF2B1	IO	LVDS7n		41	L3	M4			
B1	VREF2B1	IO	LVDS6p		42	K1	N1			
B1	VREF2B1	IO	LVDS6n		43	L1	N2			
B1	VREF2B1	IO	LVDS5p		44	L2	M6			
B1	VREF2B1	IO	LVDS5n		45	M1	N7			
B1	VREF2B1	IO	LVDS4p		46	N1	N5			
B1	VREF2B1	IO	LVDS4n		47	M2	N6			
B1	VREF2B1	IO	LVDS3p		48	N2	N3	DQ0L4	DQ0L4	DQ1L4
B1	VREF2B1	IO	LVDS3n		49	M3	N4	DQ0L5	DQ0L5	DQ1L5
B1	VREF2B1	IO	DPCLK0		50	L5	P5	DQS1L	DQS1L	DQS1L
B1	VREF2B1	VCCIO1			51					

Pin Information for the Cyclone™ EP1C12 Device
Version 1.4

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B1	VREF2B1	GND			52					
B1	VREF2B1	IO	LVDS2p		53	M4	P2	DQ0L6	DQ0L6	DQ1L6
B1	VREF2B1	IO	LVDS2n		54	N3	P3	DQ0L7	DQ0L7	DQ1L7
B1	VREF2B1	IO	VREF2B1		55	K5	R1			
B1	VREF2B1	IO			56	L4	P4			
B1	VREF2B1	IO	LVDS1p		57	R1	R2			
B1	VREF2B1	IO	LVDS1n		58	P2	R3			
B1	VREF2B1	IO	LVDS0p		59	P3	T2			
B1	VREF2B1	IO	LVDS0n		60	N4	T3			
B4	VREF2B4	IO	LVDS102p		61	R2	U3			
B4	VREF2B4	IO	LVDS102n		62	T2	V4			
B4	VREF2B4	IO	LVDS101p		63	R3	M8			
B4	VREF2B4	IO	LVDS101n		64	P4	N8			
B4	VREF2B4	IO	LVDS100p		65	R4	T4			
B4	VREF2B4	IO	LVDS100n		66	T4	U4			
B4	VREF2B4	IO	LVDS99p		67	R5	T5	DQ1B7	DQ1B7	DQ1B7
B4	VREF2B4	IO	LVDS99n		68	P5	U5	DQ1B6	DQ1B6	DQ1B6
B4	VREF2B4	GND			69					
B4	VREF2B4	VCCIO4			70					
	VREF2B4	GND			71					
	VREF2B4	VCCINT			72					
B4	VREF2B4	IO	DPCLK7		73	M5	R4	DQS1B	DQS1B	DQS1B
B4	VREF2B4	IO	VREF2B4		74	M6	R5			
B4	VREF2B4	IO	LVDS98p		75	N5	V6			
B4	VREF2B4	IO	LVDS98n		76	N6	U6	DQ1B5	DQ1B5	DQ1B5
B4	VREF2B4	IO	LVDS97p		77	P6	P6	DQ1B4	DQ1B4	DQ1B4
B4	VREF2B4	IO	LVDS97n		78	R6	P7			
B4	VREF2B4	IO	LVDS96p		79	M7	T6			
B4	VREF2B4	IO	LVDS96n				R6			
	VREF2B4	GND			80					
	VREF2B4	VCCINT			81					
B4	VREF2B4	IO	LVDS95p		82	T6	U7			DQ1B3
B4	VREF2B4	IO	LVDS95n		83	R7	V7			DQ1B2
B4	VREF2B4	IO	LVDS94p		84	P7	T7			DQ1B1
B4	VREF2B4	IO	LVDS94n		85	N7	R7			DQ1B0
B4	VREF1B4	IO	LVDS93p		86	R8	U8			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B4	VREF1B4	IO	LVDS93n		87	T8	V8			
B4	VREF1B4	IO	LVDS92p		88	M8	T8			
B4	VREF1B4	IO	LVDS92n				R8			
	VREF1B4	GND			89					
	VREF1B4	VCCINT			90					
B4	VREF1B4	GND			91					
B4	VREF1B4	VCCIO4			92					
B4	VREF1B4	IO	LVDS91p				U9			
B4	VREF1B4	IO	LVDS91n				V9			
B4	VREF1B4	IO	LVDS90p			N8	R9			DM1B
B4	VREF1B4	IO	LVDS90n			P8	T9			
B4	VREF1B4	IO	LVDS89p				M9			
B4	VREF1B4	IO	LVDS89n				N9			
B4	VREF1B4	IO	VREF1B4		93	M10	P9			
B4	VREF1B4	IO	LVDS88p				U10			
B4	VREF1B4	IO	LVDS88n				V10			
B4	VREF1B4	IO	LVDS87p		94	R9	T10	DM1B	DM1B	
B4	VREF1B4	IO	LVDS87n		95	T9	R10			
	VREF1B4	GND			96					
	VREF1B4	VCCINT			97					
B4	VREF1B4	IO					P10			
B4	VREF1B4	IO	LVDS86p		98	P9	R11			
B4	VREF1B4	IO	LVDS86n		99	N9	T11			
B4	VREF1B4	IO	LVDS85p		100	R10	U11			DM0B
B4	VREF1B4	IO	LVDS85n		101	T11	V11			
B4	VREF1B4	GND								
B4	VREF1B4	VCCIO4								
B4	VREF1B4	IO	LVDS84p			N10	V12			
B4	VREF1B4	IO	LVDS84n			P10	U12			
	VREF0B4	GND			102					
	VREF0B4	VCCINT			103					
B4	VREF0B4	IO	LVDS83p			R11	T12			DQ0B7
B4	VREF0B4	IO	LVDS83n			P11	R12			DQ0B6
B4	VREF0B4	IO	LVDS82p				V13			DQ0B5
B4	VREF0B4	IO	LVDS82n				U13			DQ0B4
B4	VREF0B4	IO	LVDS81p				T13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B4	VREF0B4	IO	LVDS81n				R13			
B4	VREF0B4	IO	LVDS80p		104	N11	N10			
B4	VREF0B4	IO	LVDS80n		105	N12	M10			
B4	VREF0B4	IO			106	M9	P12			
B4	VREF0B4	IO	VREF0B4		107	M11	P13			
B4	VREF0B4	IO	DPCLK6		108	M12	U14	DQS0B	DQS0B	DQS0B
	VREF0B4	GND			109					
	VREF0B4	VCCINT			110					
B4	VREF0B4	GND			111					
B4	VREF0B4	VCCIO4			112					
B4	VREF0B4	IO	LVDS79p		113	P12	T14	DQ1B3	DQ1B3	DQ0B3
B4	VREF0B4	IO	LVDS79n		114	R12	R14	DQ1B2	DQ1B2	DQ0B2
B4	VREF0B4	IO	LVDS78p		115	T13	V15	DQ1B1	DQ1B1	DQ0B1
B4	VREF0B4	IO	LVDS78n		116	R13	U15	DQ1B0	DQ1B0	DQ0B0
B4	VREF0B4	IO	LVDS77p		117	R14	N11			
B4	VREF0B4	IO	LVDS77n		118	P13	M11			
B4	VREF0B4	IO	LVDS76p		119	T15	U16			
B4	VREF0B4	IO	LVDS76n		120	R15	T15			
B3	VREF2B3	IO	LVDS75n		121	N13	T16			
B3	VREF2B3	IO	LVDS75p		122	P14	T17			
B3	VREF2B3	IO	LVDS74n		123	P15	R17			
B3	VREF2B3	IO	LVDS74p		124	R16	R18			
B3	VREF2B3	IO	LVDS73n		125	N15	R15	DQ1R7	DQ1R7	DQ1R7
B3	VREF2B3	IO	LVDS73p		126	N16	R16			
B3	VREF2B3	IO	VREF2B3		127	K12	P16			
B3	VREF2B3	IO			128	K14	P17	DQ1R6	DQ1R6	DQ1R6
B3	VREF2B3	GND			129					
B3	VREF2B3	VCCIO3			130					
B3	VREF2B3	IO	DPCLK5		131	L12	P15	DQS1R	DQS1R	DQS1R
B3	VREF2B3	IO	LVDS72n		132	N14	P14	DQ1R5	DQ1R5	DQ1R5
B3	VREF2B3	IO	LVDS72p		133	M13	N14	DQ1R4	DQ1R4	DQ1R4
B3	VREF2B3	IO	LVDS71n		134	M14	N18			
B3	VREF2B3	IO	LVDS71p		135	L13	N17			
B3	VREF2B3	IO	LVDS70n		136	M15	N13			
B3	VREF2B3	IO	LVDS70p		137	M16	N12			
B3	VREF2B3	IO	LVDS69n		138	L14	N16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B3	VREF2B3	IO	LVDS69p		139	L15	N15			
B3	VREF2B3	IO	LVDS68n		140	L16	M18			
B3	VREF2B3	IO	LVDS68p		141	K16	M17			DQ1R3
B3	VREF2B3	IO	LVDS67n				M14			DQ1R2
B3	VREF2B3	IO	LVDS67p				M15			DQ1R1
B3	VREF2B3	IO					M16			DQ1R0
B3	VREF2B3	GND			142					
B3	VREF2B3	VCCIO3								
B3	VREF1B3	IO	LVDS66n				L18			
B3	VREF1B3	IO	LVDS66p				L17			
B3	VREF1B3	IO	LVDS65n				M13			
B3	VREF1B3	IO	LVDS65p				L13			
B3	VREF1B3	IO	LVDS64n				L16			DM1R
B3	VREF1B3	IO	LVDS64p				L15			
B3	VREF1B3	IO					L14			
B3	VREF1B3	IO	PLL2_OUTn		143	K15	K16			
B3	VREF1B3	IO	PLL2_OUTp		144	J16	K15			
B3	VREF1B3	CONF_DONE		CONF_DONE	145	K13	K17			
B3	VREF1B3	nSTATUS		nSTATUS	146	J13	L12			
B3	VREF1B3	TCK		TCK	147	J14	K18			
B3	VREF1B3	TMS		TMS	148	J15	K14			
B3	VREF1B3	TDO		TDO	149	H15	K13			
	VREF1B3	GNDG_PLL2			150	J12	J18			
	VREF1B3	GNDA_PLL2			151	J11	K12			
B3	VREF1B3	CLK3	LVDSCLK2n		152	H16	J16			
B3	VREF1B3	CLK2	LVDSCLK2p		153	G16	J15			
	VREF1B3	VCCA_PLL2			154	H11	J12			
B3	VREF1B3	TDI		TDI	155	H14	J17			
B3	VREF1B3	IO	VREF1B3		156	H12	J14			
B3	VREF1B3	IO	LVDS63n				J13			
B3	VREF1B3	IO	LVDS63p				H13			DM0R
B3	VREF1B3	IO	LVDS62n				H14			
B3	VREF1B3	IO	LVDS62p				H15			
B3	VREF1B3	IO	LVDS61n				H16			
B3	VREF1B3	IO	LVDS61p				H17			
B3	VREF0B3	GND								

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B3	VREF0B3	VCCIO3			157					
B3	VREF0B3	IO					H18			DQ0R7
B3	VREF0B3	IO	LVDS60n				G18			DQ0R6
B3	VREF0B3	IO	LVDS60p				G17			DQ0R5
B3	VREF0B3	IO	LVDS59n		158	G14	G13	DM1R	DM1R	DQ0R4
B3	VREF0B3	IO	LVDS59p		159	G13	G14			
B3	VREF0B3	IO	LVDS58n		160	G15	G15			
B3	VREF0B3	IO	LVDS58p		161	F16	G16			
B3	VREF0B3	IO	LVDS57n		162	F14	G12			
B3	VREF0B3	IO	LVDS57p		163	F13	F12			
B3	VREF0B3	IO	LVDS56n		164	F15	F18			
B3	VREF0B3	IO	LVDS56p		165	E16	F17			
B3	VREF0B3	IO	LVDS55n		166	E15	F13			
B3	VREF0B3	IO	LVDS55p		167	D16	F14			
B3	VREF0B3	IO	LVDS54n		168	D15	F16			
B3	VREF0B3	IO	LVDS54p		169	E14	F15	DQ1R3	DQ1R3	DQ0R3
B3	VREF0B3	IO	DPCLK4		170	F12	E17	DQS0R	DQS0R	DQS0R
B3	VREF0B3	GND			171					
B3	VREF0B3	VCCIO3			172					
B3	VREF0B3	IO	LVDS53n		173	E13	E16	DQ1R2	DQ1R2	DQ0R2
B3	VREF0B3	IO	LVDS53p		174	D14	E15	DQ1R1	DQ1R1	DQ0R1
B3	VREF0B3	IO			175	H13	D18	DQ1R0	DQ1R0	DQ0R0
B3	VREF0B3	IO	VREF0B3		176	G12	E14			
B3	VREF0B3	IO	LVDS52n		177	B16	D16			
B3	VREF0B3	IO	LVDS52p		178	C15	D15			
B3	VREF0B3	IO	LVDS51n		179	C14	C17			
B3	VREF0B3	IO	LVDS51p		180	D13	D17			
B2	VREF0B2	IO	LVDS50n		181	B15	C16			
B2	VREF0B2	IO	LVDS50p		182	A15	B16			
B2	VREF0B2	IO	LVDS49n		183	B14	G11			
B2	VREF0B2	IO	LVDS49p		184	C13	F11			
B2	VREF0B2	IO	LVDS48n		185	B13	B15	DQ0T0	DQ0T0	DQ0T0
B2	VREF0B2	IO	LVDS48p		186	A13	A15	DQ0T1	DQ0T1	DQ0T1
B2	VREF0B2	IO	LVDS47n		187	B12	C15	DQ0T2	DQ0T2	DQ0T2
B2	VREF0B2	IO	LVDS47p		188	C12	D14	DQ0T3	DQ0T3	DQ0T3
B2	VREF0B2	VCCIO2			189					

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B2	VREF0B2	GND			190					
	VREF0B2	VCCINT			191					
	VREF0B2	GND			192					
B2	VREF0B2	IO	DPCLK3		193	E12	B14	DQS0T	DQS0T	DQS0T
B2	VREF0B2	IO	VREF0B2		194	E11	C14			
B2	VREF0B2	IO			195	E9	E13			
B2	VREF0B2	IO	LVDS46n		196	D12	G10			
B2	VREF0B2	IO	LVDS46p		197	D11	F10			
B2	VREF0B2	IO	LVDS45n				B13			
B2	VREF0B2	IO	LVDS45p				A13			
B2	VREF0B2	IO	LVDS44n				D13			DQ0T4
B2	VREF0B2	IO	LVDS44p				C13			DQ0T5
B2	VREF0B2	IO	LVDS43n			C11	D12			DQ0T6
B2	VREF0B2	IO	LVDS43p			B11	C12			DQ0T7
	VREF0B2	VCCINT			198					
	VREF0B2	GND			199					
B2	VREF1B2	IO	LVDS42n			A11	B12			
B2	VREF1B2	IO	LVDS42p			B10	A12			
B2	VREF1B2	VCCIO2								
B2	VREF1B2	GND								
B2	VREF1B2	IO	LVDS41n		200	C10	C11			
B2	VREF1B2	IO	LVDS41p		201	D10	D11			
B2	VREF1B2	IO	LVDS40n		202	A9	B11			
B2	VREF1B2	IO	LVDS40p		203	B9	A11			DM0T
B2	VREF1B2	IO					E11			
	VREF1B2	VCCINT			204					
	VREF1B2	GND			205					
B2	VREF1B2	IO	LVDS39n		206	D9	C10	DM0T	DM0T	
B2	VREF1B2	IO	LVDS39p		207	C9	D10			
B2	VREF1B2	IO	LVDS38n				B10			
B2	VREF1B2	IO	LVDS38p				A10			
B2	VREF1B2	IO	VREF1B2		208	E10	E10			
B2	VREF1B2	IO	LVDS37n				G9			
B2	VREF1B2	IO	LVDS37p				F9			
B2	VREF1B2	IO	LVDS36n			C8	D9			DM1T
B2	VREF1B2	IO	LVDS36p			D8	C9			

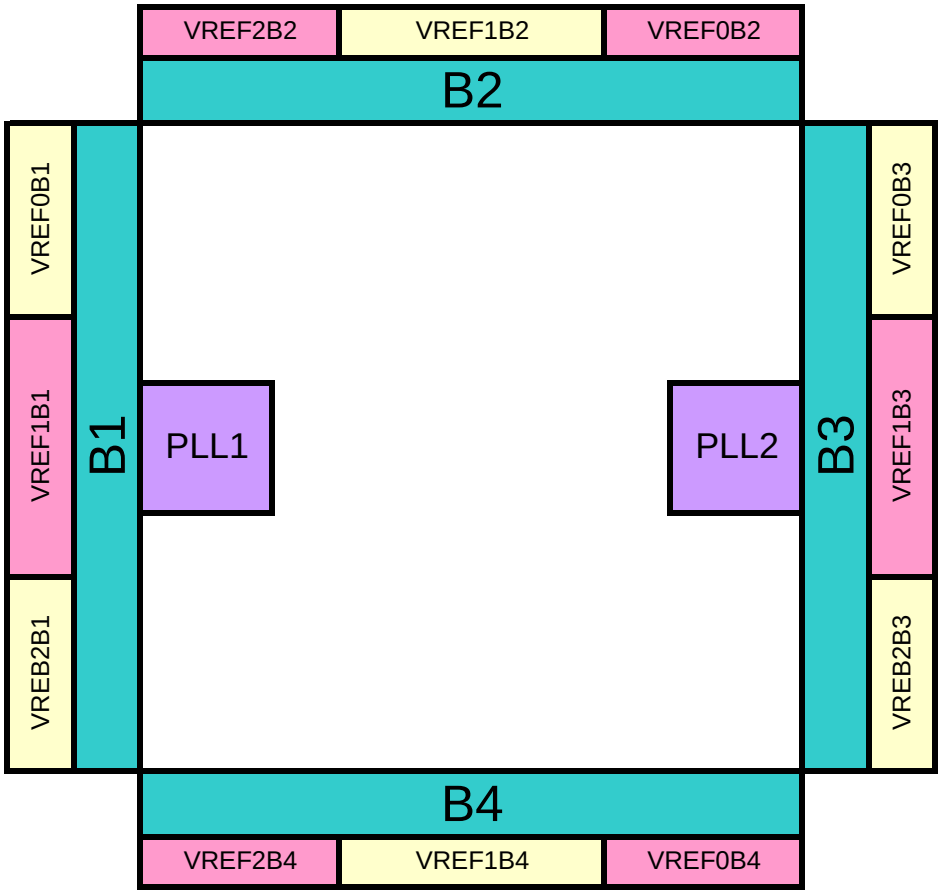
Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
B2	VREF1B2	IO	LVDS35n				A9			
B2	VREF1B2	IO	LVDS35p				B9			
B2	VREF1B2	VCCIO2			209					
B2	VREF1B2	GND			210					
	VREF1B2	VCCINT			211					
	VREF1B2	GND			212					
B2	VREF1B2	IO	LVDS34n				D8			
B2	VREF1B2	IO	LVDS34p		213	E8	C8			
B2	VREF1B2	IO	LVDS33n		214	A8	A8			
B2	VREF1B2	IO	LVDS33p		215	B8	B8			
B2	VREF2B2	IO	LVDS32n		216	D7	E8			DQ1T0
B2	VREF2B2	IO	LVDS32p		217	C7	E7			DQ1T1
B2	VREF2B2	IO	LVDS31n		218	B7	A7			DQ1T2
B2	VREF2B2	IO	LVDS31p		219	A6	B7			DQ1T3
	VREF2B2	VCCINT			220					
	VREF2B2	GND			221					
B2	VREF2B2	IO	LVDS30n				D7			
B2	VREF2B2	IO	LVDS30p		222	E7	C7			
B2	VREF2B2	IO	LVDS29n		223	B6	E6			
B2	VREF2B2	IO	LVDS29p		224	C6	D6			
B2	VREF2B2	IO	LVDS28n		225	D6	B6			
B2	VREF2B2	IO	LVDS28p		226	D5	C6			
B2	VREF2B2	IO	VREF2B2		227	E6	A6			
B2	VREF2B2	IO	DPCLK2		228	E5	B5	DQS1T	DQS1T	DQS1T
	VREF2B2	VCCINT			229					
	VREF2B2	GND			230					
B2	VREF2B2	VCCIO2			231					
B2	VREF2B2	GND			232					
B2	VREF2B2	IO	LVDS27n		233	C5	C5	DQ0T4	DQ0T4	DQ1T4
B2	VREF2B2	IO	LVDS27p		234	B5	D5	DQ0T5	DQ0T5	DQ1T5
B2	VREF2B2	IO	LVDS26n		235	A4	A4	DQ0T6	DQ0T6	DQ1T6
B2	VREF2B2	IO	LVDS26p		236	B4	B4	DQ0T7	DQ0T7	DQ1T7
B2	VREF2B2	IO	LVDS25n		237	C4	F8			
B2	VREF2B2	IO	LVDS25p		238	B3	G8			
B2	VREF2B2	IO	LVDS24n	DEV_OE	239	A2	B3			
B2	VREF2B2	IO	LVDS24p	DEV_CLRn	240	B2	C4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
		VCCINT				A7	A17			
		VCCINT				A10	A2			
		VCCINT				G8	B1			
		VCCINT				G10	B18			
		VCCINT				H7	H10			
		VCCINT				H9	J9			
		VCCINT				J8	K10			
		VCCINT				J10	L9			
		VCCINT				K7	U1			
		VCCINT				K9	U18			
		VCCINT				T7	V17			
		VCCINT				T10	V2			
		VCCIO1				C1				
		VCCIO1				G6	E1			
		VCCIO1				P1	G7			
		VCCIO1					M7			
		VCCIO1					P1			
		VCCIO4				T3				
		VCCIO4				L7	P11			
		VCCIO4				L10	P8			
		VCCIO4				T14	V14			
		VCCIO4					V5			
		VCCIO3				P16				
		VCCIO3				K11	E18			
		VCCIO3				C16	H12			
		VCCIO3					M12			
		VCCIO3					P18			
		VCCIO2				A14				
		VCCIO2				F10	A14			
		VCCIO2				F7	A5			
		VCCIO2				A3	E12			
		VCCIO2					E9			
		GND				A1	A1			
		GND				A16	A16			
		GND				A5	A18			
		GND				A12	A3			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	Q240	F256	F324	DQS for x8 in the Q240	DQS for x8 in the F256	DQS for x8 in the F324
		GND				F6	B17			
		GND				F8	B2			
		GND				F9	C1			
		GND				F11	C18			
		GND				G7	H11			
		GND				G9	H8			
		GND				G11	H9			
		GND				H8	J10			
		GND				H10	J11			
		GND				J7	J8			
		GND				J9	K11			
		GND				K6	K8			
		GND				K8	K9			
		GND				K10	L10			
		GND				L6	L11			
		GND				L8	L8			
		GND				L9	T1			
		GND				L11	T18			
		GND				T1	U17			
		GND				T5	U2			
		GND				T12	V1			
		GND				T16	V16			
		GND					V18			
		GND					V3			

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	No connect pins should not be connected on the board. They should be left floating.
	Configuration and JTAG Pins	
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.
	Clock and PLL Pins	
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin.
PLL2_OUTp	I/O, Output	External clock output from PLL 2. This pin can be used with differential or single ended I/O standards. If clock output from PLL2 is not used, this pin is available as a user I/O pin.
PLL2_OUTn	I/O, Output	Negative terminal for external clock output from PLL2. If the clock output is single ended, this pin is available as a user I/O pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..102]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 102. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDS[0..102]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 102. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin.
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.



Notes:

1.This is a top view of the silicon die.

2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

Bank & PLL Diagram

Version Number	Date	Changes Made
1.4	3/6/2006	Added CRC_ERROR pin in Pin List and Pin Definitions